Digital Domain Feature Detection in a Complex Dielectric Sensor

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Abstract

An existing industrial sensor is used to monitor the production of synthetic polymer fiber, by measuring changes as fiber passes through an electromagnetic field. Dedicated analog circuitry performs low-level processing to detect specific physical structures in the fiber. Measurement of a given fiber requires fine-tuning of the analog circuitry, so the sensor cannot be configured to optimally measure multiple fiber types.

It is proposed that the analog circuitry be replaced by a digital equivalent, using digital signal processing techniques where applicable. This will facilitate a less complex calibration procedure and allow real-time sensor parameterization. Effectiveness will be evaluated against the existing analog sensor, in terms of speed, accuracy, cost, and power consumption.

1 Introduction

An existing complex dielectric sensor (hereafter referred to as 'sensor') is the basis for a real-time synthetic polymer fiber monitoring system. The sensor measures variations in fiber as it passes through an electromagnetic field, in the form of a magnitude and phase reading. These readings provide a measure of fiber density and composition.

Multi-filament synthetic fibers often contain structural features called nodes. A node is a section of fiber where filaments have been knotted in order to prevent fiber separation. Among other characteristics, the sensor has been designed to detect the frequency and quality of fiber nodes. This functionality is implemented via dedicated analog circuitry, which derives node information based on raw sensor readings.

2 Motivation

Fiber composition, operation temperature, and sensor location within the manufacturing process are the primary factors affecting signal input range. For a given application and fiber type, this range can vary significantly. Obtaining useful data often requires measurement of fiber variations that are significantly less than 1 pF. As a result, careful calibration is required to ensure that the fiber will stay within the input range while at the same time maximizing sensitivity.

The calibration procedure requires a high-precision network analyzer and manual adjustment of a number of potentiometers. On average, the existing procedure requires 12 hours to complete calibration for a single sensor. For a typical installation, several hundred (or thousand) person-hours are required to prepare sensors for field operation. Clearly, this is a time-consuming and costly process. In the event that calibrated values do not match the fiber input range, the sensor must be removed from production and sent back to the factory for re-calibration.

To reduce the likelihood of this problem, it is desirable to have the capability to modify sensor calibration parameters without physical interaction. One method to achieve this is to implement the analog hardware

in the digital domain. Calibration parameters can then be updated via software, based on the type of fiber to be analyzed. The proposed approach is to capture data (using an analog-to-digital converter) prior to performing any signal processing. Data is to be processed in the digital domain, using digital signal processing (DSP) techniques to model the analog processing circuitry. The intent is not to eliminate the calibration procedure, but to simplify it. This approach assumes that fiber input does not exceed the physical limitations of the sensor.

3 Design Constraints

Modeling analog circuitry in the digital domain presents some challenges. A sophisticated information system is built around data collected from fiber sensors. Minor changes in sensor data may have significant implications on system performance. To reduce the risk of a negative impact, the behaviour of a digital implementation should ideally match that of the existing analog circuitry (with the exception of improved calibration).

A digital realization is constrained by the capabilities of the digital signal processor and supporting hardware. Incoming data is known to be band-limited at approximately 15 kHz, which implies a minimum 30 kHz sampling rate in order to satisfy the Nyquist criteria [1]. To prevent aliasing, magnitude and phase signals must be sampled at or above this rate. In addition, each sensor can accommodate up to four channels. As a result, a digital solution must process data at no less than 240 kHz.

Assuming the technical constraints for speed and accuracy can be realized, cost is the primary constraint. To be feasible, a digital solution must cost less than the current implementation. The number of required components is expected to reduce by 50% - 75%. This may reduce the number of circuit boards required by the sensor, and production costs (including manufacturing and components costs) are expected to decline. The primary cost reduction measure is a simplified calibration procedure, which has the potential to significantly reduce costs associated with preparing and maintaining sensors.

Power consumption is another important factor, as it has a direct influence on cost. The addition of a digital signal processor will likely result in increased power demands, despite the reduction in analog components. Sensors are powered via an external 24 V power supply. Industrial wiring regulations require that the supply lines are fused at 4 A, which limits the number of sensors that can be powered by a single power supply. To maintain the power supply-to-sensor ratio, a digital implementation must not exceed existing power demands by more than 15%. Power consumption will be affected by choice of processor as well as how efficiently the circuitry can be modeled in software [2].

4 Feature Detection

The feature detection circuitry is primarily responsible for extracting information related to nodes (frequency and quality). As fiber, under tension, passes through the electromagnetic field, it generates a magnitude signal. When a node passes through the field, the compressed fiber shape results in a reduced response, causing a decrease in signal level. A graphical representation of the node detection procedure is outlined in Figure 1. Note that noise has been removed from the signal for illustration purposes.

Node detection is based on variations of the magnitude signal around the DC level (refer to Figure 1). A node begins when the magnitude drops below the DC level. When the signal rises above DC, a fixed-length node count pulse is generated to indicate a valid node. Node quality is a measure of how tightly a node is knotted, and is directly proportional to the peak-to-peak magnitude reading as a node occurs.

The node circuitry incorporates several parameters to detect valid nodes. In particular, node duration must fall within a specified range, and the node quality reading must exceed a pre-defined minimum value.

Some of these parameters can be adjusted via potentiometers, while others are set at time of manufacture via RC component selection. Note that this is a simplified view of how node detection is performed [3].

The sensor also includes a self-calibration mechanism, which is invoked at regular time intervals. During these intervals, valid input data is interrupted and node processing is disabled. Because of this, node information for these periods must be interpolated. Currently, these operations are performed in software, further down the information processing chain.

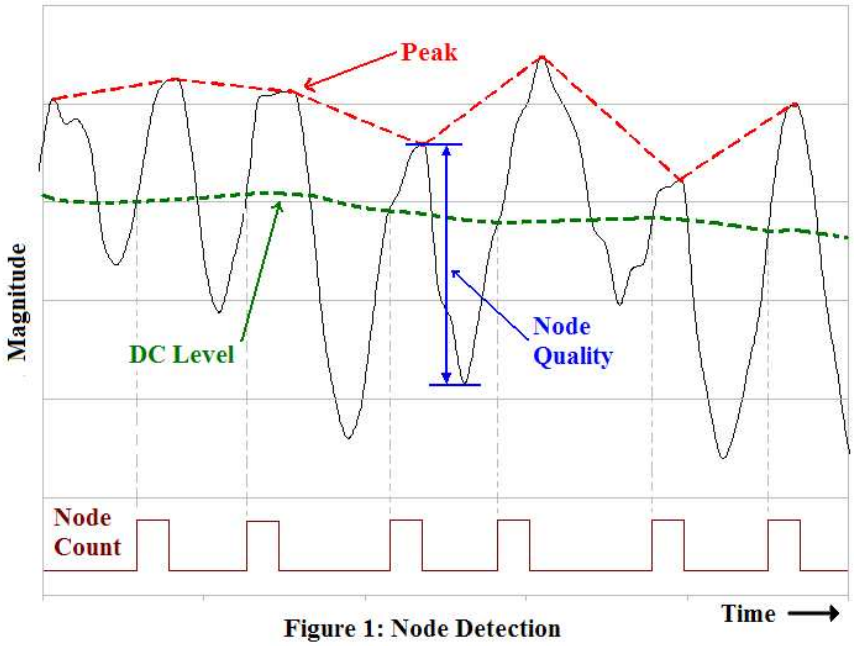

Figure 1: Node Detection

5 Design Approach

To facilitate digital implementation, the existing analog circuitry has been broken down into smaller functional blocks. The proposed approach is to model the behaviour of each block in software, and then assemble the blocks into a working design. One advantage of this approach is that existing design documents can be used to validate the (digital) design. In addition, the risk of significantly altering output data with respect to the analog design is reduced.

In order to reduce development time and cost, a proof-of-concept will be developed using a commercially available DSP development kit. Initially, the function of the analog circuitry will be modeled for one channel. If the speed of this model is adequate, the design will be extended to multiple channels, thereby reducing cost.

The design will be subject to the DSP platform chosen. The initial (generic) implementation is expected to be inefficient relative to processor capabilities. Most signal processors incorporate architectural features to improve performance of operations that are commonly used in DSP. By tweaking the design, it may be possible to achieve better performance relative to a specific processor. Once the design is verified, investigation will proceed into adding additional functionality (see Future Work).

6 Design Verification

The proof-of-concept is meant to serve as a baseline for performance evaluation. Once complete, the design must be verified. To accomplish this, an existing (analog-based) sensor will be used, with data originating from real-world synthetic fiber. The digital implementation can be setup to run simultaneously, using the same data. Assuming the processor can manage the data with adequate speed, a direct comparison can be made between the analog and digital outputs.

For this application, filter design appears to be the most significant contributor to algorithm performance, both in terms of speed and accuracy. In particular, the difference between the analog and digital implementations are expected to primarily be a result of filter discrepancies. A filter chosen for computational efficiency may not provided the desired frequency response (and vice versa). Where applicable, discrepancies in output between analog and digital representations will be analyzed using high-level software such as Matlab.

As a prototype, it will be difficult to evaluate parameters such as cost and power consumption. Additional components may be required to support the DSP processor, including a mechanism to download and store calibration or algorithm parameters. Some approximations can be made for both cost and power consumption using the techniques described in [4] and [5]. A more involved analysis will be possible when the prototype is incorporated as part of a fully functional sensor.

7 Implementation

The proof-of-concept has been under development, using a 16-bit, fixed-point DSP development kit in conjunction with a multi-channel analog-to-digital conversion module capable of 250 kHz sampling. A function generator was used to provide a simulated node signal in the form of a sinusoid. A single channel has been modeled in the digital domain. To speed development, relative simple constructs were used where possible, to be refined later.

An example of starting with a simple construct and moving to a more complex design can be seen in the implementation of a DC blocking filter, which is required prior to evaluating node information. The first implementation attempted to subtract the DC offset from the original signal via a simple boxcar FIR filter. However, the FIR filter required more memory than was immediately available. Reducing the filter size provided an increase operational speed, but with an unacceptable reduction in accuracy. Subsequently, the filter was refined to use less memory (using an IIR approach), which significantly improved performance [6]. The resulting DC level was suitably matched with the DC offset of the input signal.

At the time of publication, the digital version of the (single channel) node detection algorithm is capable of running at 260 kHz. The next design stage is to extend the single channel effort to four channels and verify that the minimum 240 kHz processing target can be achieved on the development hardware. Further code optimization is expected, which should allow the algorithm to run significantly faster on the provided hardware.

8 Results

Feature detection circuitry has been digitally modeled for one channel at 260 kHz, and this has yielded some beneficial results. For example, one functional design block involves integrating a signal over a specified period of time (at which point the integrator is reset). As the analog design evolved, it was discovered that the integrator output was not always correct due to a non-zero initial level. In order to correct the problem, hardware modifications and high-level software changes were required. In the digital domain, the integrator can programmatically be set to zero, and the added hardware/software modifications become redundant. The result is a more reliable and accurate solution, which in turn reduces overall costs.

With minor changes for efficiency, the chosen DSP hardware appears capable of performing node detection at the desired operational speed. Using a digital approach, calibration values for feature detection can be controlled by software variables instead of analog potentiometers. The result is a simplified calibration procedure, which will significantly decrease sensor production and maintenance costs. Measures relating to cost and power consumption can be more closely approximated once the design is finalized.

9 Future Work

Ideally, fiber nodes should occur at regular intervals. Given that the sensor measures the number of nodes over a specific period of time, it is possible that a frequency domain analysis might yield useful results. In practice, nodes do not have an even distribution. The resulting frequency spectrum will likely contain a peak that is spread out over several frequencies. Even with this limitation, it may be possible to augment frequency-domain analysis with time-domain results, assuming sufficient processing power is available.

Further performance can often be achieved via code optimization. In the absence of specific library routines, this process requires in-depth knowledge of the underlying hardware architecture, at the cost of reduced portability [7]. The prototype hardware is based on a 16-bit fixed-point processor, for efficient integer operations. The processor supports circular addressing and single-cycle multiply-accumulate operations. In addition, there are eight internal data busses for data transfer between the ALU and on-chip memory. Once the proof-of-concept is complete, exploitation of these architectural features for efficiency will be investigated.

Additional functionality may be incorporated into the design depending on available resources. For example, the sensor is sensitive to static electricity, which can cause spikes in the data. Analog methods have been unsuccessful in removing these unwanted signals, but a digital approach may yield better results.

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