Memorial University of Newfoundland

Engineering 4862 MICROPROCESSORS

Assignment 5

Instructor: Cheng Li Due: July 20, 2005

-- Part A --

0. What control byte will configure an 8255A PPI such that Ports A & B are input, and Port C is output?

1. Sketch a diagram of an address decoder for an 8-bit input port. The assembly language instruction IN AL, 94h should fetch a byte from the port. There should be no more than 1024 mirror images, and it should not interfere with operation of I/O ports at 0010h and 0037h.

2. What is the advantage and penalty of multiplexing and demultiplexing the address/data in the 8088/86 CPUs?

3. When the input signal RESET in the 8088/86 is activated, what are the contents of the CS and IP register? Why ROM is always arranged to the high/upper end of the memory map (closer to the FFFFFH) for Intel 80x86 serial microprocessors?

4. Show the logical design of "MOV [0100], AL" for memory mapped I/O using AND and Inverter gates and a 74LS373 latch. Assume that DS=B800H.

-- Part B --

5. In the following questions, the target microprocessor is an 8088 running at 5 MHz. Assume a memory data fetch will retrieve the value 9Fh. The initial register contents are:

(CS) = 8500h (DS) = 1800h

(IP) = 0100h (AX) = 5763h (BX) = 117Dh

(a) The 8088 loads and executes the following instruction. Translate the following instructions from assembly language into machine code. Show all workings.

ADD BYTE PTR [BX], AL

(b) For the ADD instruction, determine all the contents on the address bus and data bus for all machine cycles.

(c) For the ADD instruction, draw in your answer book a detailed timing diagram showing all execution bus cycles (that is, those cycles involved with reading or writing data bytes). Assume that there are no wait states.

Include the following signals: CLK, all address and data, IO/M*, ALE, RD*, and WR*. Clearly indicate the T-states, and label the type of each full bus cycle.

6. Calculate, using execution times, the total time required by the following program. Assume the program is running on a system with 5-MHz 8086 microprocessor (with the help of Intel User Manual).

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MOV AX, 0000h
MOV SI, 0000h
MOV CX, 8000h
OUTER: MOV DX, CX
MOV [SI], AX
ADD SI, 2
MOV CX, 0FFFFh
INNER: LOOP INNER
MOV CX, DX
LOOP OUTER
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7. Repeat the previous question for a system with a 4.77-MHz 8088 microprocessor. (Only recalculate values that change.)

8. Is it possible to create an 8086-based computer system with one 32KB (8-bit wide) RAM device and one 16KB (8-bit wide) RAM device? Explain.

9. (**Bonus Question**) An 8086-1 microprocessor based system operating in minimum mode at its maximum speed already includes 4 kilobytes of RAM (two 2K x 8 devices) and 16 kilobytes of EPROM (two 8K x 8 devices), which are mapped in appropriate locations with no mirror images. This system needs to be expanded by adding two 51256S-10 SRAM devices and one 27210-200V10 EPROM device. A new address decoder should be added which would cater to the expansion devices; the most significant three address lines with one 74LS138 should be used for this purpose.

a. *Assuming that the data lines needs to be buffere*d, sketch a circuit diagram illustrating the interface between the CPU and the expansion memory. Show all the connections to the pins of the memory devices; include latches and all the necessary TTL devices. The existing memory devices (4K RAM and 16K ROM) and their address decoders **need not** be included in your diagram.

b. List the address ranges (for both ROM and RWM) corresponding to all memory devices in the system – existing as well as additional devices. List all mirror images.

c. Sketch the memory map of the system – including the existing as well as newly added memory – and clearly indicate all mirror images.

d. Consider the address line A13. Find out the additional load – current as well as capacitance load – placed on this line due to the expansion. Which device should be capable of driving this additional load?

e. Determine the number of wait states required to interface the (i) SRAM and the (ii) EPROM. Suggested propagation delays are: decoder ~40ns, latch ~30ns, buffer ~25ns, transceiver ~30ns, and each logic gate ~10ns.

f. Assume that the O4* output line of the decoder in your design is used for selecting a pair of memory mapped 8255 PPI devices. Assume also that Port A in both these devices have been configured as input, thus obtaining a 16-bit input port. What address(es) should be used to access this 16-bit port?

g. Write a program that will read the contents of this port at a known sampling rate, and store the acquired information in an array located in the expansion RAM; 100 samples are required to be collected. Hint: use the extra segment for the RAM.

h. Suppose that the rate at which samples are collected is not pre-determined, but depends on the speed of the input device connected to the 8255. Therefore, you cannot simply write a delay routine to determine when to collect input samples. What hardware/software solution would you recommend to solve this problem? That is, how will you use the 8255 device in this case?