ENG 4862 MICROPROCESSORS

Spring 1996 FINAL EXAMINATION

Memorial University of Newfoundland
St.John's Canada A1B 3X5

August 9, 1996 Friday 9 to 11.30 AM. :: X-2043 :: RV

Clearly *state your assumptions*, if any. Answer all questions. Write all your answers in the *answer book*. INTEL handbooks may be used. Text books and class notes are not allowed.

Enclosed are the ASCII table and extracts from data sheets of the following devices: 8088 Microprocessor, 74LS138 Decoder, Am9232 UV-EPROM, and MCM6208C SRAM.

100+6 : Total Marks

0. State why the following are not valid instructions in 8086/88 assembly language:

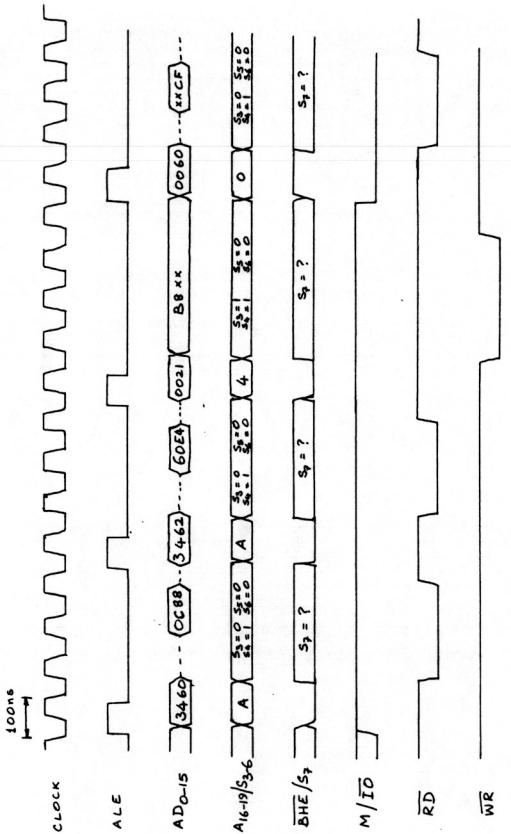
   (a) AND SS:[BX+SI], 37CH
8 (b) SUB CX, [AX+23]
   (c) OUT 2AH, AH
   (d) PUSH AL

1. Suppose that a programmable timer device has to be added to an 8088-based computer such that the timer causes a *type 12h* interrupt every one second. Explain how this can
8 be accomplished. Assume that the timer has already been programmed to generate an appropriate signal every one second, and that the interrupt service routine corresponding to the timer is loaded into the memory starting at FE840h.
2. Sketch the waveform on the data line of a serial communication interface when '*b*' (lower
8 case) is transmitted with one stop bit and space parity at 4800 baud/sec. Assume that logic high corresponds to -12 V and logic low to +12 V. Calculate the time required to fill a screen which has 80 characters per line and 24 lines per screen.
3. Discuss briefly the functions of the following devices in an 8086-based minimum mode system:
8 a) DMA Controller
   b) 74LS373 Octal transparent negative edge-triggered D-latch with tristate buffer.

4. BONUS: We know that an I/O device can be I/O mapped or memory mapped in an Intel 8086/8088 microprocessor based system, also understand the implications of both
(4) alternatives. Similary, a memory device can be either memory mapped or I/O mapped. Discuss the effects of I/O mapping a memory device.

5. Study carefully the attached timing diagram. This diagram contains waveforms of certain
(29+2) signals in a system based on an Intel microprocessor.

2 a) Which microprocessor is used in the system? How can you determine this?
2 b) What is the clock speed and the crystal speed of the system?
2 c) How many bus cycles are represented in this diagram? How can you determine this?
3 d) Describe in words the contents of the READY line during these bus cycles.
   e) What type of bus cycle is each of them? Looking at the status lines, determine if
5 any of these are opcode fetch bus cycles. Hint: Find out the Segment used.
2 f) If (CS) = A000, determine the contents of the instruction pointer at the start of these bus cycles.
   g) Explain what is accomplished by the system during these bus cycles. Assume the following register contents. (DS):4000, (ES):A000, (SS):2000, (AX):ED6A,
8 (BX):407B, and (DX):44AE.
2 h) Looking at the data bus contents determine the contents of the CPU registers SI and CL.
2 i) What are the final contents of AX and DX?
(2) j) BONUS: Supposing an interrupt request arrives at the INTR input pin sometime during one of these bus cycles, what will be the consequence?



6. An **8088-2** microprocessor operating in minimum mode at 6 MHz clock speed employs Am9232B EPROM and MCM6208C SRAM devices to obtain at least 3 kilobytes of read-only memory (ROM) and at least 20 kilobytes of read-write memory. In addition to these, there are a few peripheral devices the interface design of which is **not included** in this question. (40)

a) Sketch a circuit diagram of the memory interface. Use **one** 74LS138 decoder device. Show all the connections to the pins of the memory devices. Your diagram *need not* include the clock generator, latches, buffers or the circuitry required to generate control signals other than the device select lines. 8

b) How many mirror images are there for each device? Substantiate your answer. Ensure that your system can be initialized. 5

c) Consider the address line A9. Find out the current as well as the capacitance load on this line. Assume the load due to I/0 ports totals 50 μA (both for logic low and high) and 20 pF. Based on this load, determine if it is necessary to buffer this address line. 8

d) Assume that the data lines are buffered. Determine the number of wait states, if any, required to interface the EPROM. Suggested propagation delays are: Decoder: 45ns, Latch (with buffer): 35ns, Buffer: 25ns, Transceivers: 30ns and simple gates (OR, NOT, etc.): 5ns. 8

e) Three different speed versions of the RAM device are available. Which one would you choose in this design, and why? 4

f) Write an assembly language subroutine which reads one byte from RAM and outputs this to a storage oscilloscope through an I/O mapped Digital to Analog Converter (DAC). This operation should be repeated as frequently as possible for a certain total duration (known to be less than 50 milliseconds). At every step, the RAM location situated below the previous one should be used. Assume the port address of the DAC to be 5CD8H. 7