Engineering 4862 Microprocessors

Spring 1997 Final Examination

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EN2043

Comments:

Clearly state your assumptions, if any. Answer 5 out of 6 questions in Part I; answer all questions in Part II. Write your answers in the answer book. Intel handbooks may be used. Text books and class notes are not allowed. Unless stated otherwise, a reference to a CPU or microprocessor indicates an Intel 8088 or Intel 8086.

Enclosed are data sheets for the Motorola MCM6290B 16K x 4 SRAM, the Intel 2732A 4K x 8 UV EPROM, the 8254 Programmable Interval Timer and the 8255 Programmable Peripheral Interface.

100 (+5 bonus) marks

5 pages

Part I   Short Answer Questions   35 marks

Answer 5 of the following 6 questions.

7   1.   If a manufacturer states that the capacity of a particular RAM IC is 64K, how many bytes of information can it store? What other pieces of information are needed to determine the number of address lines?

List the key differences between an SRAM IC and a DRAM IC. How does a system address a memory element on a DRAM IC? Be sure to include a reference to any additional lines the DRAM requires.

7   2.   Suppose an 82C54 programmable interval timer has a 2 MHz clock entering the CLK 0 input. What count value is needed to generate a pulse (Mode 2) every 5 ms? If the timer was mapped to I/O addresses A0H to A3H, write the necessary instructions to configure the timer counter 0 (including control word and count value).

7   3.   To set the register AX to 0, the most logical instruction to use is **MOV AX, 0**. However, there are two other commonly used instructions that perform the same operation. One is **SUB AX, AX**, and the other is **XOR AX, AX**. Do two comparisons, one on the basis of execution times and one using machine cycles, to determine which is the fastest method for an **8088**-based system. Assume that the instructions have already been loaded for the execution time analysis.

Why is it not possible to use the subtraction or the exclusive-or methods if the destination is a memory location?

7   4.   What is memory mapped I/O? For an 8-bit output port, the following address line values are used to access it using memory mapping:

```
AB19                                            AB0
1 0 X X   X X X X   X X 0 0   0 0 0 0   0 1 1 1
```

How many mirror images does this device have? Give an instruction to output the value **80H** to this output port using the register BX as the offset and ES as the segment. Give a set of sample values for both BX and ES to access this port.

7   5.   What are the sequence of events when a hardware non-maskable interrupt occurs? What memory locations are used by the CPU to determine the location of the interrupt service routine? Assuming the service routine is located at F300:25A2, give the values of each byte at these original memory locations.

7   6.   How many T1 cycles are in the following partial timing diagram? Does the second bus cycle
               contain 4 or 5 clock cycles (*careful*)? Explain your reasoning, and include an explanation of the
               appearance of the extra clock cycle.
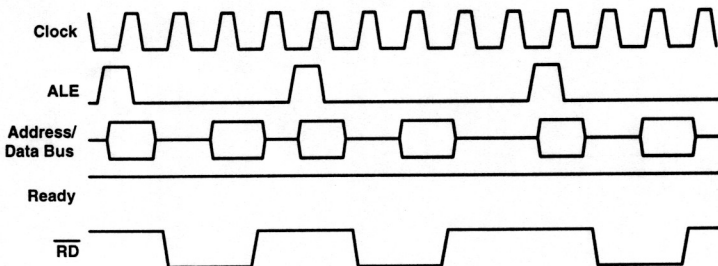
+5   *BONUS QUESTION*
               Modern microprocessors, such as the Intel Pentium or the Motorola PowerPC 604e, are clocked at
               two different rates. The fastest speed is the internal clock of the CPU, at which instructions are
               executed. An external clock is provided for the buses, and determines how fast data and code can
               be transferred between the CPU and memory. The internal clock speed is an integer multiple of the
               external clock.

               Based on your knowledge of pipelining, which might be the faster computer system: a system with
               a 233MHz CPU and a 33MHz bus, or a system with a 200MHz CPU and a 50MHz bus? Explain.

Part II Design/Analysis Questions   **65 marks**
Answer **both** questions 7 and 8.

(25) 7. The following three instructions are located one after another, in the given order, starting at the memory location specified by the **8086** register contents:

$(CS) = F200$, $(DS) = 4000$, $(ES) = 2A00$, $(SS) = 4600$, $(IP) = 15BA$
$(AX) = 1997$, $(BX) = 0600$, $(CX) = 9ABC$, $(DX) = 73E8$
$(BP) = 02A0$, $(SP) = 1000$, $(SI) = FF00$, $(DI) = 10A5$

```
PUSH AX
MOV  AX, [BX+DI]
OUT  50H, AX
POP  AX
```

11 (a) Determine the contents of the **address** bus and the **data** bus during each (fetch as well as execution) bus cycle; state the **type** of each bus cycle. The execution of an instruction completes immediately after its machine code has been loaded by the CPU. Assume any unknown data with non-trivial values.

10 (b) Only for the execution bus cycle of the MOV instruction, sketch a timing diagram to show the following signals of the 8086: clock, ALE, address / data / status lines, BHE*/S7, RD*, WR*, and M / IO*. Assume that the memory device requires **one wait state**. Show the contents on each of the bus lines, except for the status lines. Assume minimum mode operation.

4 (c) Determine the contents of IP, SP, and AX immediately after the execution of these instructions. What flags have been affected by these instructions, if any?

(40)   8.   An **8088-1** microprocessor based system operating in minimum mode with a 24MHz crystal will be used to create a Model Railroad control system. The system will employ the Motorola MCM6290B-35 16K x 4 SRAM and the Intel 2732A-25 4K x 8 UV EPROM. You may use **one** 74LS138 (3 x 8 decoder with eight active low outputs, two active low enable inputs, and one active high enable input) for the address decoding. This microprocessor has been tested with a load capacitance of 100pF.

It is necessary for the system to have at least 16KB of RAM and 10KB of ROM, with at least some RAM and ROM mapped to the appropriate memory locations. You may have any number of mirror images for the memory devices; memory does not need to be contiguous. The system should be designed using minimum essential support devices.

2   (a)   How many memory devices (both RAM and ROM) are needed?

10   (b)   Assuming that the data lines do **not** need to be buffered, sketch a circuit diagram illustrating the interface between the CPU and the memory. Show all the connections to the pins of the memory devices; include latches and all the necessary TTL devices. You **need** to generate the control signals for both memory and I/O devices. Do **not** show the connections to the 8284 clock generator IC. Be careful to use the pins for the correct SRAM.

6   (c)   List the address ranges for all memory devices in the system; list all mirror images.

4   (d)   Consider the multiplexed address / data line AD9. Find out the current as well as capacitance load on this line when the microprocessor drives it with address information. Assume that the load due to I/O ports totals 45 µA (both for logic low and logic high) and 20 pF. Based on this load, determine if it is necessary to buffer this address line.

8   (e)   Determine if wait states are required to interface the EPROM. Propagation delays are about 40 ns for the decoder, 30 ns for the latch, 30 ns for transceivers, and 10 ns for each SSI device (OR and NOT gates). **Briefly** state the effect of using a slightly slower clock crystal.

10   (f)   The system also contains both an 8255 Programmable Peripheral Interface (PPI) IC (address range 60H to 63H) and an 8254 Programmable Interval Timer (PIT) IC (address range 70H to 73H).

On the PPI chip, Ports A and C are configured for output, and Port B is configured for input (all for simple I/O - Mode 0). Bit 0 of Port A is used to turn on (value 1) or off (value 0) flashing red lights at a road crossing. Bits 0 and 1 on Port B are both used to detect if a train is approaching or at the crossing - a value of 1 on either bit means that the train is present.

The *PCLK* output from the 8284 clock generator IC is connected to *CLK0* on the PIT IC, and *OUT0* is connected to *CLK1*. *OUT1* is ORed with bit 0 of Port A and connected to a signal crossing light. The frequency of *OUT1* should be 1 Hz, and should be a square wave (Mode 3).

Write an ***assembly-language routine*** to control the signal crossing. Only when a train is detected should the lights flash. Your code needs to initialize both chips, and contain a main loop which activates or de-activates the lights (you may use an infinite loop). You may assume that bits 1 to 7 of Port A are not connected to any other device. You must comment your code!