Instructor: Cheng Li, licheng@mun.ca, EN - 4012, 737-8972
Office Hours: Monday 14:00 – 16:00, or by individual appointment
Lectures: Tuesday, and Thursday 14:30 - 15:45 in EN - 1001
Labs: Thursday 9:00 - 12:00 in EN - 3065
Objective: This course aims to cover concepts, tools, and issues pertaining to specification, modeling, analysis, simulation, testing and synthesis of digital systems, including PLD, FPGA, and ASIC devices.
Prerequisites: Knowledge about Digital Logic Circuits, OOP, and Microprocessors.
Contents: The topics will include, but not be limited to:
2. Advanced Minimization Techniques
3. Design of Logic Circuits with Programmable Logic Devices (PLDs, FPGAs)
4. Introduction to ASICs and ASIC Design Methodology
5. Analysis, Modeling and Partitioning for Logic Synthesis and VHDL Coding
6. Constraining Designs, Synthesizing, Simulation and Optimization
7. Design for Testability, Built-In Self-Test, and Fault Tolerance
8. Digital System Reliability
9. Noise and Transmission Line Effects
Evaluation: Problem sets (4): 0 % (Due: Jan. 25, Feb. 8, Mar. 15, Mar. 31)
Labs and mini-project: 30 %
Midterm: 20 % (March 1st, Tuesday, tentative)
Final exam: 50 %
Teaching Assistants: Cheng Wang Office: EN-2041 E-mail: cwang@mun.ca
References: