Engineering 5865 Digital Systems

Problem Set 1

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0. The question deals with minimization in digital circuit.
    a) What are the advantages of minimizing digital circuits?
    b) List the usual procedures employed to minimize the sequential as well as the combinational parts of digital circuits.
    c) Discuss why minimization is approached differently while realizing the control unit.

1. Consider the following function F along with don't care conditions
    F(A, B, C, D) = A'B'C'D + A'BC'D' + ABC + AB'C'D' + ABCD'
    D(A, B, C, D) = $\sum$(0, 2, 5, 6, 7, 10, 11)

    Assume normal as well as complement of all the input variables are available in all the following sections.
    a) Show that F = BC + A'C' + B'D' is a logically correct solution.
    b) Identify the static hazard(s) in this realization.
    c) Implement this expression using only 2-input NAND gates.
    d) Using Karnaugh map, derive another expression for F, which corresponds to a circuit without a static hazard.
    e) Realize F obtained in d) using not more than three 2-input gates. Assume NAND, NOR, XOR, AND, and OR gates are available.
    f) Realize F using only NOR gates (having any numbers of inputs).
    g) Realize F using a decoder that has active low outputs and an active low enable input, plus another gate (having any number of inputs).
    h) Minimize F using postulates and theorems in Boolean algebra. Justify each step.

2. Using master-slave D flip-flops and multiplexers, design a 4-bit right shift register that has the following features: a synchronous parallel load, a synchronous clear, and a hold. An asynchronous clear is not required.

3. Describe the pins and the internal arrangement of a 4M x 8 memory device.

4. Booth recording is a popular algorithm to realize multiplication of 2's complement signed binary numbers. The algorithm works as follows: Let A be the n-bit multiplier, and B the n-bit multiplicand. Initialize an n-bit number, P, that is concatenated with another n-bit number. Consider two adjacent bits of the multiplier at a time, starting with the least significant bit. If these two bits are equal to each other, then P is unchanged. Assume $A_{-1} = 0$. If $A_i = 0$ and $A_{i-1} = 1$, then P ← P + B; if $A_i = 1$ and $A_{i-1} = 0$, then P ← P – B. In any case, shift right ARITHMETIC the 2n-bit number by one bit position – that is, the sign bit is always the serial Right In bit. This process is repeated until the most significant bit of the multiplier is considered. Remember that all are 2's complement signed binary numbers, and so all additions and subtractions should be done following the corresponding rules.

    a) Verify the algorithm by multiplying -3 and -5.
    b) Design the datapath and a controller for a Booth recording 32-bit multiplier. A block diagram, with all modules appropriately labeled and all connections between modules clearly identified, as well as an ASM chart will be adequate.
    c) Discuss the changes that would be required to the unsigned multiplication algorithm. Compare the hardware complexities resulting from these two methods.

5. The following state table describes a digital system.
    a) Is this a Mealy or Moore machine? Why?
    b) Reduce the number of states to the fewest possible number and demonstrate that only two flip-flops are required to realize this system. Show all steps.
    c) Realize the system using negative edge triggered T flip-flops and necessary gates.
    d) What would be required to initialize the system to a particular state?
    e) Is your realization self-starting? Why?
    f) Complete the timing diagram on the sheet provided to you, assuming that the system start in state e or an equivalent state.

Present State	Next State		Output	
	Input x=0	Input x=1	Input x=0	Input x=1
a	a	b	0	0
b	e	c	0	1
c	c	d	1	0
d	a	b	0	0
e	b	d	0	0
f	f	a	1	0
g	e	f	0	1
h	g	d	0	0