

Engineering 5865 Digital Systems

Problem Set 2

0. List all the transactions in the following description. Use Synopsys or Mentor Graphics simulator to verify your answer from this and other questions.

```
ARCHITECTURE concurrent OF timing_demo IS
    SIGNAL a, b, c : BIT := '0';
BEGIN
    a <= '1' AFTER 2 NS;
    b <= NOT a AFTER 3 NS;
    c <= NOT b AFTER 4 NS;
END concurrent;
```

1. List all the transactions in the following description.

```
ARCHITECTURE sequential OF timing_demo IS
    SIGNAL a, b, c : BIT := '0';
BEGIN
    PROCESS ( )
    BEGIN
        a <= '1';
        b <= NOT a;
        c <= NOT b;
        WAIT;
    END PROCESS;
END sequential;
```

2. Given the following signal assignments, show all transactions placed on each signal. At each event, show transactions that are appended, overwritten, and expired. Show resulting waveforms on each signal. This question requires a qit overload NOT operator.

```
ARCHITECTURE dataflow OF signals IS
    TYPE qit IS ('0', '1', 'Z', 'X');
    SIGNAL a, b, c : qit := '0';
BEGIN
    a <= NOT a AFTER 10 NS WHEN NOW <= 30 NS;
    b <= 'Z', a AFTER 25 NS, '0' AFTER 35 NS;
    c <= '1', a AFTER 5 NS, b AFTER 20 NS;
END dataflow;
```

3. Your company is planning to start manufacturing a new device that contains two thousand flipflops and tens thousand gates. The volume of production is expected to be around half a million devices per annum. Would you go for a full-custom ASIC or a PLD / FPGA? Discuss in detail for your reason.
4. Using several instances of the 2-input NOR gate supplied below, write an entity declaration and a gate-level architecture for a 5-input NOR gate. Remember that NOR is not an associative operator.

```
ENTITY nor2 IS
    PORT (i1, i2: IN BIT; o1: OUT BIT);
END nor2;
```

5. The following is a synthesizable VHDL code for a *puzzle* circuit.

```
ENTITY puzzle IS
    PORT (a, b: IN std_logic_vector (3 DOWNTO 0); c_in: IN
          std_logic_vector (2 DOWNTO 0);
          c_out: OUT std_logic_vector (2 DOWNTO 0));
END puzzle;
```

```
ARCHITECTURE dataflow OF puzzle IS
BEGIN
```

```
    c_out <= "100" WHEN a > b ELSE "001" WHEN b > a ELSE c_in;
END dataflow
```

- a) Explain what exactly will be implemented in hardware. In other words, what component is being implemented by this code?
 - b) Comment on the > operator employed in this architecture.
6. Design a 16-bit left / right shift register with synchronous parallel load and an active-low asynchronous clear input using the D flip-flop and 4×1 MUX provided below as components. Show the function table of the shift register. Write VHDL code for the shift register, including entity and a structural architecture. A modular design would simplify the code!

```
ENTITY d_ff IS
    PORT (d, clrbar, clk : IN BIT; q, qb : OUT BIT);
END d_ff;
```

```
ENTITY mux_4x1 IS
    PORT (i1, i2, i3, i4, s0, s1 : IN BIT; o1 : OUT BIT);
END mux_4x1;
```

7. Using the tabular (Quine-McCluskey or prime implicants chart) method, minimize the following Boolean expressions:
 - a) $F(A, B, C, D, E) = \sum (4, 6, 7, 9, 11, 12, 13, 14, 15, 20, 22, 25, 27, 28, 30) + d (1, 5, 29, 31)$
 - b) $F(U, V, W, X, Y, Z) = \sum (0, 4, 8, 16, 24, 32, 34, 36, 37, 39, 40, 48, 50, 56)$.