Engineering 5865 Digital Systems

Problem Set 3

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0. Write a dataflow description for a 1-bit subtractor. Include a borrow input and a borrow output. Construct a 4-bit serial subtractor by using the 1-bit subtractor as the primitive component. Write the structural level description for the 4-bit subtractor. Write the testbench code which can be used to test the 4-bit subtractor.

1. Using the style of the serial adder that provided below, write a behavioral description for a serial subtractor. Indicate the changes you will make so that the testbench you have written can be to test this behavioral level serial subtractor.

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ENTITY serial_adder IS
      PORT (a, b, start, clock : IN BIT; ready : OUT BIT;
             result : BUFFER BIT_VECTOR (7 DOWNTO 0));
END serial_adder;

ARCHITECTURE behavioral OF serial_adder IS
BEGIN
      PROCESS (clock)
             VARIABLE count : INTEGER := 8;
             VARIABLE sum, carry : BIT;
      BEGIN
             IF (clock = '0' AND clock'EVENT) THEN
                    IF start = '1' THEN
                           count := 0;
                           carry := '0';
                    ELSE
                           IF count < 8 THEN
                                  count := count + 1;
                                  sum := a XOR b XOR carry;
                                  carry := (a AND b) OR (a AND carry) OR (b AND carry);
                                  result <= sum & result (7 DOWNTO 1);
                           END IF;
                    END IF;

                    IF count = 8 THEN
                           ready <= '1';
                    ELSE
                           ready <= '0';
                    END IF;
             END IF;
      END PROCESS;
END behavioral;
```

2. The value of a signal called 'SOUR' should be assigned to another signal called 'DEST' so that there is a lag of 100 ns between the two. However, if signal SOUR experiences a change for a duration less than 85 ns, then signal DEST should not follow this change. Write the VHDL statement that will accomplish this.

3. Design a synchronous sequential circuit that detects overlapping 101 sequences on an input line. Sketch a state diagram corresponding to this detector. Employ negative edge triggered J-K flip-flops and any simple gates. Note that if the input sequence is 000101111001101010110, the output sequence must be 000001000000001010100. Design this as a Moore machine. Write the VHDL code

4. Given the following description, show waveforms on $x1$, $x2$, and diff signals in a timing diagram. Explain the reason for the difference on $x1$ and $x2$.

    ARCHITECTURE comparing OF findout IS
        SIGNAL c, $x1$, $x2$, $diff$: BIT := '0';
    BEGIN
        c <= '0', '1' AFTER 60 NS, '0' AFTER 120 NS;
        $x1$ <= '1' AFTER 6 NS WHEN c'EVENT ELSE $x1$;
        $x2$ <= '1' AFTER 6 NS WHEN NOT c'STABLE ELSE $x2$;
        $diff$ <= $x1$ XOR $x2$;
    END comparing;

5. Use a process statement to develop a behavioral description for a toggle flip-flop (t-ff). The t_ff has a single t input and two q and qb outputs. After the rising edge of the t input, the two outputs will be complemented. The q output has a low-to-high propagation delay of q_tplh and a high-to-low propagation delay of q_tphl. The nq output has a low-to-high propagation delay of qb_tplh and a high-to-low propagation delay of qb_tphl. Pass the propagation delays as generic parameters and use them in your behavioral description. Write the complete description using the entity declared below:

    ENTITY t_ff IS
        GENERIC ($q\_tplh, q\_tphl, qb\_tplh, qb\_tphl$: TIME);
        PORT (t : IN BIT; q, qb : OUT BIT);
    END t_ff;