Instructor: Cheng Li, licheng@engr.mun.ca, EN - 4012, 737- 8972
Office Hours: Monday, Wednesday 12:00 - 13:00, or by appointment
Lectures: Tuesday, and Thursday 10:30 - 11:45 in EN - 1003
Labs: Thursday 14:00 - 17:00 in EN - 3065
Objective: This course aims to cover concepts, tools, and issues pertaining to specification, modeling, analysis, simulation, testing and synthesis of digital systems, including PLD, FPGA, and ASIC devices.
Prerequisites: Knowledge about Digital Logic Circuits, OOP, and Microprocessors.
Contents: The topics will include, but not be limited to:
2. Advanced Minimization Techniques
3. Design of Logic Circuits with Programmable Logic Devices (PLDs, FPGAs)
4. Introduction to ASICs and ASIC Design Methodology
5. Analysis, Modeling and Partitioning for Logic Synthesis and VHDL Coding
6. Constraining Designs, Synthesizing, Simulation and Optimization
7. Design for Testability, Built-In Self-Test, and Fault Tolerance
8. Digital System Reliability
9. Noise and Transmission Line Effects

Evaluation: Problem sets (4): 0 %
Labs and miniproject: 30 %
Midterm: 25 % (Feb 27th, Tuesday, tentative)
Final exam: 45 %

Teaching Assistants:
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Computer-Aided Design Tools:
Synopsys, Mentor Graphics, and Cadence CAD Tools for Digital System VLSI Design
References: