Engineering 9865 Advanced Digital Systems

Problem Set #4

(Due: March 18, 2016)

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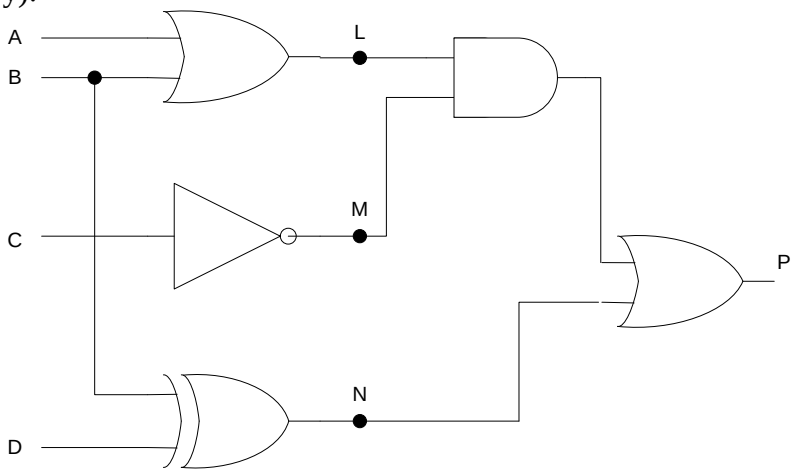
0. This question deals with selection of Application-Specific Integrated Circuits.
   a. Discuss in detail factors to be considered when one has to select between developing a semi-custom (FPGA or PLD) ASIC device and a full-custom (CMOS) ASIC device.
   b. Small PLD devices (such as the PAL device you used in the lab) are relatively inexpensive compared to large ones that cost thousands of dollars each. It is highly probable to make an error while designing larger chips (one containing thousands of gates and flip-flops). So, it will not be advisable to use one-time programmable devices; furthermore, any enhancement or adaptation to changing environment would be difficult to cope with. State the solution usually employed to solve this problem.

1. A company is planning to start manufacturing a new device that contains two thousand flip-flops and tens thousands gates. The volume of production is expected to be around half a million devices per annum. Would you go for a full-custom or a semi-custom ASIC? Discuss in detail reasons for your choice.

2. The following Boolean functions correspond to 3-input 4-output combinational problem. Tabulate the PAL programming table for the circuit and make the fuses to be shown in the PAL device ash shown in the next sheet.

   A (x,y,z) = Σ(1, 4, 6) + d (2),
   B (x,y,z) = Σ (0, 3, 6, 7) + d (1, 5),
   C (x,y,z) = Σ (1, 2, 6, 7) + d (4),
   D (x,y,z) = Σ (1, 2, 3, 5, 7).

3. Consider the following simple combinational logic circuit. Using path sensitization procedure generate the necessary (minimum number of) test patterns to ensure that any single stuck-at-0 and stuck-at-1 fault at the intermediate points L, M, and N will be detected (location of faults is not necessary).



4. This question deals with testing.
   a. What is the objective of testing a VLSI chip that has been fabricated?
   b. What is the fault model normally assumed in testing? How does this relate to defects in the circuit? Why is it all right to assume that multiple faults do not occur?
   c. If you determine certain internal faults are untestable, what can be done to improve the situation?
   d. What is the usual procedure to make a sequential circuit testable?

5. Discuss in detail the measures that can be taken to minimize the effect of noise in a mobile robot that has a wireless link with a PC, and employs several photo, capacitance and thermal transducers. This robot is used for mining operations.

6. A digital system, referred to as System A, is constructed using 100 components of type X and 200 components of type Y. A second digital system, referred to as System B, is constructed of 150 components of type X and 50 components of type Y.
   a. If the MTTF of System A is 3 years, and the MTTF of System B is 5 years, what are the failure rates of each component in FITs?
   b. If a third digital system C is constructed using 143 components of type X and 78 components of type Y, what is the reliability of this system C after 10 years?
   c. Discuss the implicit assumption(s) used in the quantitative analysis here.

7. The manufacturer of an MSI IC package specifies that the device features a constant failure rate of 200 failures in billion hours.
   a. When would the constant failure rate assumption be valid?
   b. What is the mean time to failure (MTTF) of the device in years?
   c. If a system is put together with five such components, what are the chances that the system will be functioning without any device failures one year after development? Assume all five components must work for the system to function properly.
   d. Suggest how the reliability of the system using these devices could be further improved?
   e. What would be required to make this a highly available system?

8. This question deals with transmission line effect.
   a. Explain how reflections could occur at both ends of a transmission line.
   b. How can these reflections affect the performance of a digital circuit?
   c. What can the system designer do to avoid this problem?
   d. What is the maximum length of the transmission line for which one can guarantee this problem will not occur?
   e. Calculate the reflection coefficients when the characteristic impedance is 150 ohms, source resistance is 75 ohms and terminating resistance is 450 ohms.

9. An electronic monitor consisting of analog and digital circuits is located next to a HVDC transmission tower somewhere between Churchill Falls and St. Anthony. This equipment includes sensors (for measuring temperature, wind, and humidity), necessary electronics, a Pentium IV PC and a modem. Recommend ways of designing this system to minimize the effects of noise.