§ 4 Programmable Logic Devices (PLD)

1. PLDs widely used in digital design.
2. PLDs include:
    a. ROMs (read-only memorials)
    b. PLAs (programmable logic arrays)
    c. PALs (Programmable array logic)
3. More complex
    a. FPGA (field programmable gate arrays)
    b. CPLD (Complex Programmable Logic Devices)

§ 4.1 ROMs

1. Consists of an array of semiconductor devices interconnected to store an array of binary data.
2. Can't be changed once burned in.
3. Conceptually, consist of a decoder and a memory array.

§ 4.2 PLAs

1. A PLA with n inputs and m outputs can realize m functions of n variables.
2. Difference from ROM:
    a. Decoder → An AND array that realizes selected products terms of the input variables
    b. OR array → Ors together the product terms needed to form the output functions.

3. Internally, the PLA uses NOR-NOR logic.
4. The added input and output inverting buffers make it equivalent to AND-OR logic.
5. Logic gates are formed in the array by connecting switching transistors between the column lines and the row lines.
6. Examples:

F0 = A'B' + AC'
F1 = B + AC'
F2 = A'B' + BC'
F3 = AC + B

§ 4.3 PALs

1. A special case of the PLA where the AND array is programmable and the OR array is fixed
2. Less expensive than the more general PLA.
3. Easier to program.

4. Widely used to replace individual logic gates.
5. Typically combinational PALs:

   10-20 inputs and 2-10 outputs

   2-8 AND gates during each OR gate

   e.g., 22V10 → 24 PINs, 22 I/O PINs, 10 output (FFs), and 12 input only.

6. Also available to have D-FF with input driven from PLA ➔ Useful to realize sequential circuits.

   E.g., Z = X.Q3' + X'.Q3

   D3 = Q1.Q2.Q3 + X'.Q1.Q3' + X.Q1'.Q2'

§ 4.4 PGAs and CPLDs

1. PLDs capable of a sequential network, but not a complete digital system.
2. PGAs, CPLDs are more flexible, versatile to implement a complete digital system on a single IC chip, even a processor.
3. Xilinx FPGAs

   Example: 3000 series FPGA XC3020

   Consists of an interior of

   64 configurable logic blocks (CLBs)

   surrounded by a ring of

   64 input-output interface blocks (IOBs)

   Each CLB contains some combinational logic and 2 DFFs.

   The interconnections between blocks can be programmed by storing data in internal configuration memory cell.

   Advanced devices are similar, but more powerful.

4. Altera CPLDs

   An extension of the PAL concept.

   Consists of a number of PAL like logic blocks together with a programmable interconnect matrix.

Each PAL-like logic blocks has a programmable AND array that feeds macro cells (basically FFs), the output of these macrocells can be routed to the inputs of the logic blocks within the IC.

Many CPLSs are electronically erasable and reprogrammable, sometimes referred to as EPLDs.

Example: MAX 7000 series.

Use EEPROM-based configuration memory cells.

Consists of Logic Array Blocks (LABs), I/O cControl Blocks, and a Programmable Interconnect Matrix (PIA).

Each LAB has 16 Macrocells, each contains combinational logic and a FF, has 36 inputs from PIA and 16 outputs to PIA. 8-16 outputs from each LAB can be routed to I/O pins through the I/O control block. 8-16 inputs from I/O pins can be routed through the I/O control block to the PIA.

§ 4.5 ASIC Design Methodology

1. Generally speaking, Top-Down Design Process followed by Bottom-up Implementation

2. During the top-down design process, top level entity is recursively divided by using the divide-and-conquer strategy until all leaf components of the design tree become manageable.

3. Factors to be considered between a semi-custom ASIC device (FPGA, PLD) and a full-custom ASIC device (CMOS IC).

   a. Speed
   b. Number of input and output pins
   c. Size of the circuit
      i. Enough FFs / Latches / Gates
      ii. Then actual mapping
   d. If constraints from CLB and IOB and interconnections between blocks are not prohibitive
      ➔ ASIC might be good option if available
   e. Number of gates < 1M
      Number of pins < a few hundreds ➔ available for FPGA and CPLD
   f. Volume of product

i. < hundreds of thousands → semi-custom
ii. > millions of devices → full-custom less expensive
iii. Always prudent to first bring out an FPGA (less development time), in the mean time full-custom ASIC

g. If involves analog → full custom normally required

4. ASIC Design flow recommended by CMC