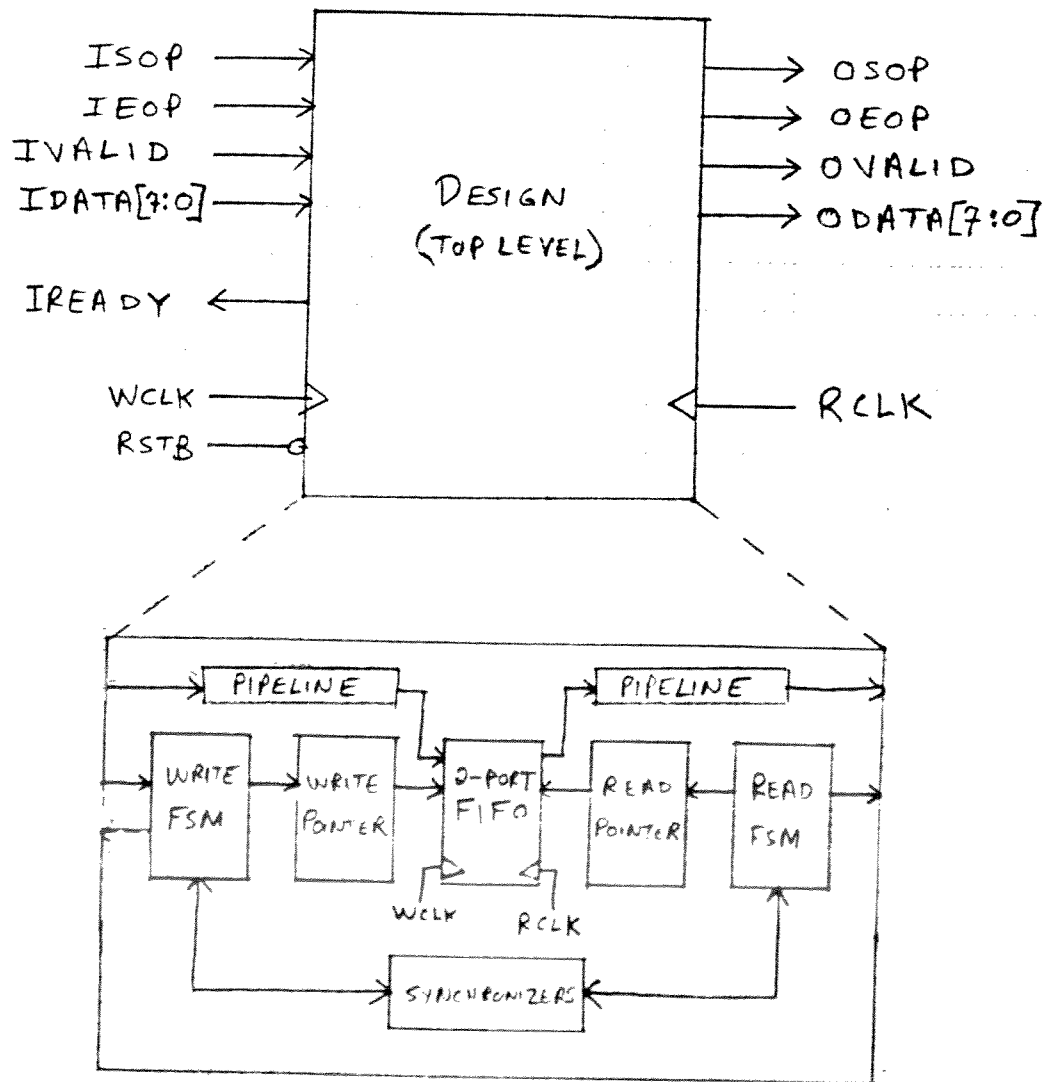# Design Project Specification

The following document provides a complete specification of the design project for this course. Throughout the lectures, assignments and labs, the components and processes required to complete this design project will be discussed. Accordingly, the assignments and labs have been structured such that their completion provides most of what's needed to complete this design project. At the end of the course, you will have designed, implemented, synthesized, functionally verified, and if time permits, inserted scan logic and generated scan vectors for the simple design specified in this document.

1. Block Diagram

Below is the block diagram for the design project.

2. I/O Description

WCLK
The write clock (WCLK) input clocks the signals on the input interface and all logic on the write side of the FIFO. WCLK is nominally a 80 MHz clock with a 50/50 duty cycle.

RCLK
The read clock (RCLK) input clocks the signals on the output interface and all logic on the read side of the FIFO. RCLK is nominally a 100 MHz clock with a 50/50 duty cycle.

RSTB
The active low reset (RSTB) input provides an asynchronous reset to all sequential logic in the design. When the RSTB input is set low, all sequential logic in the design is held in reset. When the RSTB input is set high, the design is not held in reset and operates normally. The RSTB input must be glitch free.

ISOP
The active high input start of packet (ISOP) input indicates when the first byte of packet data is present on IDATA[7:0]. The ISOP input is only valid when the IVALID input is high. When ISOP is high and IVALID is high, IDATA[7:0] contains the first byte of packet data.
ISOP is sampled on the rising edge of WCLK.

IEOP
The active high input end of packet (IEOP) input indicates when the last byte of packet data is present on IDATA[7:0]. The IEOP input is only valid when the IVALID input is high. When IEOP is high and IVALID is high, IDATA[7:0] contains the last byte of packet data.
IEOP is sampled on the rising edge of WCLK.

IVALID
The active high input valid (IVALID) input indicates that ISOP, IEOP and IDATA[7:0] are valid. When IVALID is high, ISOP, IEOP and IDATA[7:0] are valid. When IVALID is low, ISOP, IEOP and IDATA[7:0] are invalid.
IVALID is sampled on the rising edge of WCLK.

IDATA[7:0]
The input data (IDATA[7:0]) inputs contain the input packet data bytes. IDATA[7:0] contains valid data when the IVALID input is high. IDATA[7:0] contains invalid data when the IVALID input is low.
IDATA[7:0] are sampled on the rising edge of WCLK.

IREADY
The active high input ready (IREADY) output indicates that the design can accept a complete packet of data on the input interface. When IREADY is high, a packet transfer may commence on the input interface (denoted by ISOP high) in the next WCLK cycle. When IREADY is low, a packet transfer may not begin on the input interface.
IREADY must be set low 2 WCLK cycles following the start of a packet transfer on the input interface, and must remain low until the design can again accept a complete packet of data on the input interface.
Once a packet transfer has begun, for purposes of determining whether or not the next packet transfer can occur, upstream logic must wait at least 2 WCLK cycles following the end of packet transfer (denoted by IEOP high) before using the status of the IREADY output.
IREADY is updated on the rising edge of WCLK.

OSOP   The active high output start of packet (OSOP) output indicates when the first byte of
                packet data is present on ODATA[7:0]. The OSOP output is only valid when the
                OVALID output is high. When OSOP is high and OVALID is high, ODATA[7:0]
                contains the first byte of packet data.
                OSOP is updated on the rising edge of WCLK.

OEOP   The active high output end of packet (OEOP) output indicates when the last byte of
                packet data is present on ODATA[7:0]. The OEOP input is only valid when the
                OVALID output is high. When OEOP is high and OVALID is high, ODATA[7:0]
                contains the last byte of packet data.
                OEOP is updated on the rising edge of WCLK.

OVALID   The active high output valid (OVALID) output indicates that OSOP, OEOP and
                ODATA[7:0] are valid. When OVALID is high, OSOP, OEOP and ODATA[7:0] are
                valid. When OVALID is low, OSOP, OEOP and ODATA[7:0] are invalid.
                OVALID is updated on the rising edge of WCLK.

ODATA[7:0]   The output data (ODATA[7:0]) outputs contain the output packet data bytes.
                ODATA[7:0] contains valid data when the OVALID output is high. ODATA[7:0]
                contains invalid data when the OVALID output is low.
                ODATA[7:0] are updated on the rising edge of WCLK.

3. Functional Description

The primary function of the design is to move packets of data from the input interface to the output
interface through a FIFO. The input interface and output interface are clocked by different clocks that
are asynchronous to each other.

Because latency is of little importance in this design, data is moved through the FIFO in a transfer
based fashion. This means that a complete packet is written into the FIFO before any data is read from
the FIFO. And all data is read from the FIFO before any subsequent packet data is written into the
FIFO. This avoids the complex nature of designing and implementing a circular FIFO where data is
simultaneously read from one side of the FIFO while being written into the other side of the FIFO.

<u>Input Interface</u>

The input interface is a byte wide, 80 MHz interface used to transfer packet data into the FIFO. Each
packet transfer may vary from a single byte packet to a maximum of 32 bytes.

Upstream logic must provide a minimum of 2 idle clock cycles on the input interface between each
packet transfer.

Upstream logic may pause data transfer by de-asserting the IVALID signal for 1 or more clock cycles
between data bytes. However, the design has no means of throttling upstream logic during packet
transfer, and must accept all data bytes provided by upstream logic until the complete packet has been
transferred over the input interface.

Upstream logic may not begin a packet transfer until IREADY is high. Once a packet transfer has
begun, IREADY must be de-asserted within 2 clock cycles following ISOP high. IREADY must
remain de-asserted until a complete packet can again be accepted on the input interface.
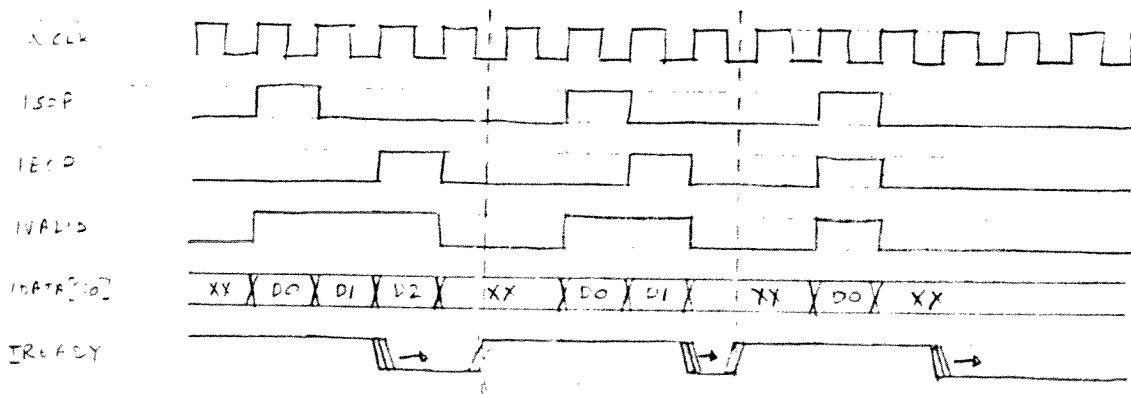
Output Interface

The output interface is a byte wide, 100 MHz interface used to transfer packet data out of the FIFO. During each packet transfer, all of the data stored in the FIFO must be provided on the output interface.

If necessary, the design may pause data transfer by de-asserting the OVALID signal for 1 or more clock cycles between data bytes. However, downstream logic has no means of throttling the design during packet transfer on the output interface, and must accept all data bytes provided by the design until the complete packet has been transferred over the output interface.

4. Functional Timing Diagrams

Below are the functional timing diagrams for the design project.

The diagram below shows 3 packets being transferred on the input interface. Note that before each packet transfer can begin, upstream logic must sample IREADY high. The first packet is a 3 byte packet. The second packet is a 2 byte packet. The third packet is a 1 byte packet. For all 3 packet transfers, there are no pauses between data byte transfers (IVALID always high). Note that the vertical dashed line represents a break in time of at least 2 clock cycles.
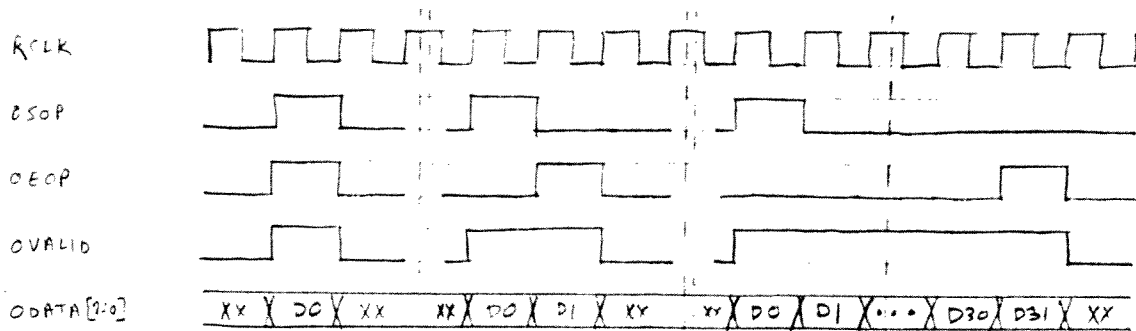

1) 3 BYTE PACKET
2) 2 BYTE PACKET
3) 1 BYTE PACKET

The diagram below shows 2 packets being transferred on the input interface. Note that before each packet transfer can begin, upstream logic must sample IREADY high. The first packet is a 3 byte packet. The second packet is a 32 byte packet. For the 3 byte packet transfer, there are pauses between data byte transfers (IVALID goes low for one or more clock cycles between data bytes). Note that the vertical dashed line represents a break in time of at least 2 clock cycles.
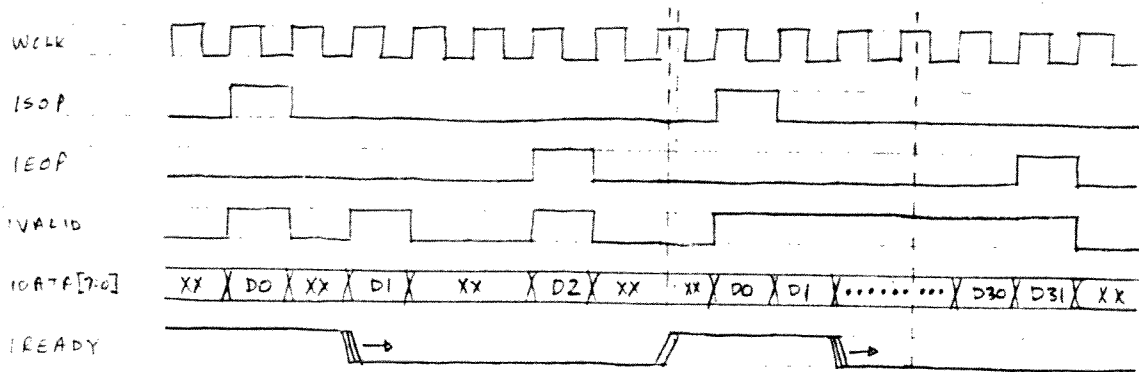
1) 3 BYTE PACKET WITH DELAYS
2) 32 BYTE PACKET (MAX PACKET SIZE)

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The diagram below shows 3 packets being transferred on the output interface. Note that downstream logic has no means of throttling data transfer, and accordingly, each data byte is output one after the other in a continuous manner (OVALID always high). The first packet is a 1 byte packet. The second packet is a 2 byte packet. The third packet is a 32 byte packet. Note that the vertical dashed line represents a break in time of at least 2 clock cycles.


1) 1 BYTE PACKET
2) 2 BYTE PACKET
3) 32 BYTE PACKET (MAX PACKET SIZE)

5. Timing Specifications

Below are the timing specification diagrams for the design project.

The diagram below shows the timing for all I/O synchronous to the write clock (WCLK). Note that the maximum frequency of WCLK is 80 MHz (12.5 ns period), and the duty cycle, although nominally 50/50, cannot exceed 40/60 or 60/40. All inputs have a minimum setup time of 3 ns, and a minimum hold time of 0 ns. All outputs have a minimum propagation delay of 0 ns, and a maximum propagation delay of 3 ns.
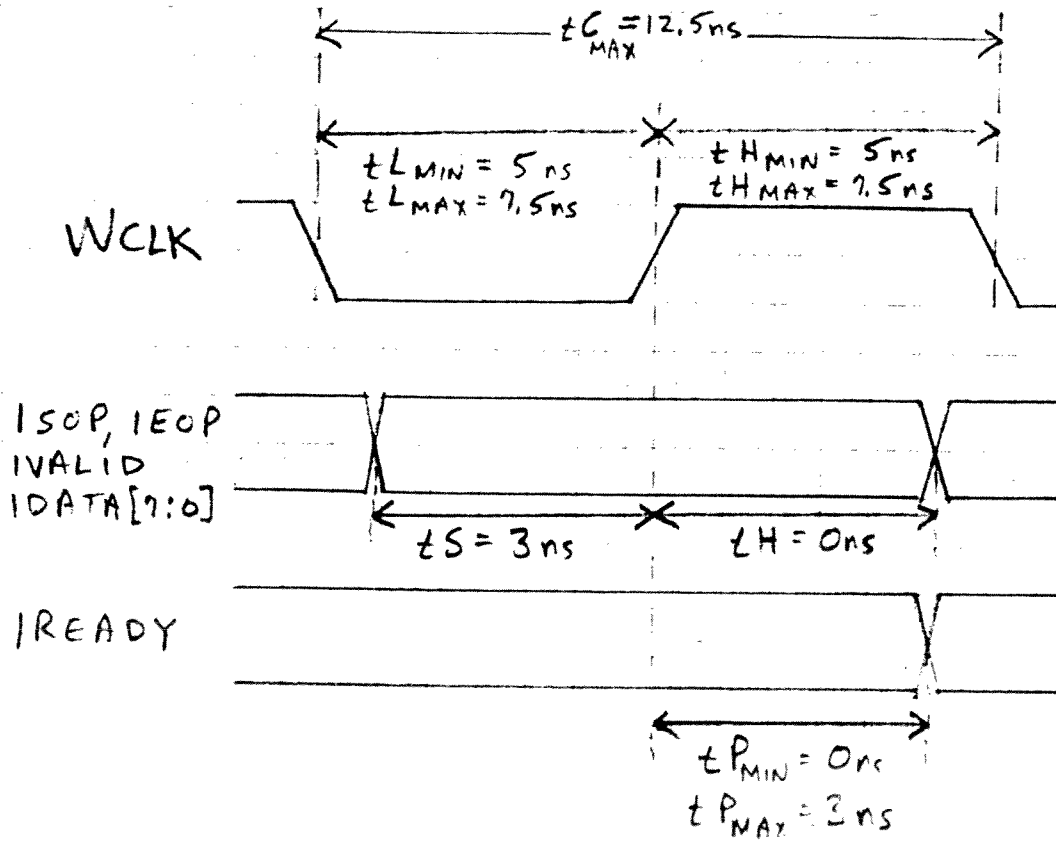
The diagram below shows the timing for all I/O synchronous to the read clock (RCLK). Note that the maximum frequency of RCLK is 100 MHz (10 ns period), and the duty cycle, although nominally 50/50, cannot exceed 40/60 or 60/40. There are no inputs on the design synchronous to RCLK. All outputs have a minimum propagation delay of 0 ns, and a maximum propagation delay of 3 ns.
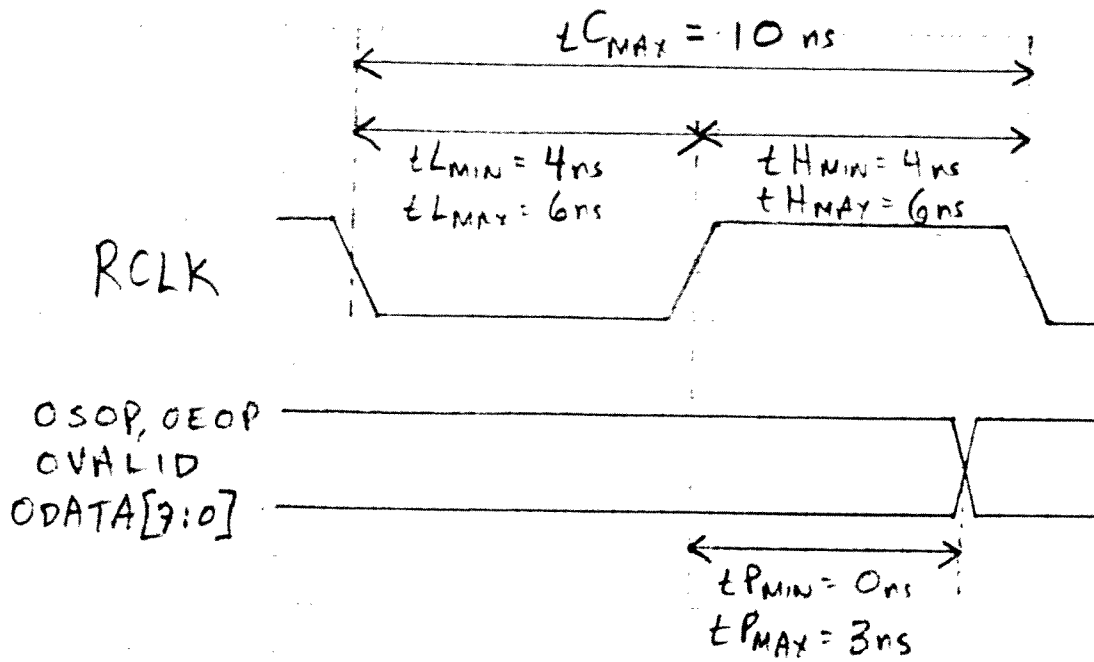
The diagram below shows that the asynchronous reset input (RSTB) must be asserted for at least 100 ns. This is identified as the minimum pulse width of the RSTB input.
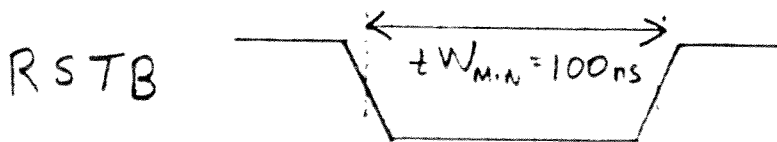
6. Electrical and Other Design Specifications

- The maximum capacitance on any net is 1.5 pF.
- The maximum transition time on any net is 1.5 ns.
- All synchronous I/O must be registered – i.e. all inputs are sampled and all outputs are retimed, and no combinational logic exists between the sampling register (FF) and the corresponding synchronous I/O port.
- All outputs must have a minimum of 7X drive strength.
- All inputs have a minimum fanout of 1, except WCLK, RCLK and RSTB, which are unbuffered.
- The maximum fanout of any net in the design is 15.
- Synthesize to minimize area.