

Memorial University of Newfoundland
Engineering 9865 Advanced Digital Systems
COURSE OUTLINE

Winter 2011

<http://www.engr.mun.ca/~licheng/9865>

Instructor:	Cheng Li, licheng@engr.mun.ca , EN - 4012, 864- 8972														
Office Hours:	Monday 14:00 - 16:00, or by individual appointment														
Lectures:	Tuesday 10:30 – 11:45, Wednesday 11:00 – 12:15 in EN - 4008														
Labs:	Thursday 14:00 - 17:00 in EN - 4033														
Objective:	This course aims to cover concepts, tools, and issues pertaining to specification, modeling, analysis, simulation, testing and synthesis of digital systems, including PLD, FPGA, and ASIC devices.														
Prerequisites:	Knowledge about Digital Logic, Microprocessors, Computer Architecture, and Object Oriented Programming,.														
Course Text:	C. Roth, <i>Digital Systems Design Using VHDL (2nd Edition)</i> , CL-Engineering Publisher, March 2007 (ISBN-10: 0534384625, ISBN-13: 978-0534384623).														
Contents:	The topics will include, but not be limited to: <ol style="list-style-type: none">1. Concepts of Digital Logic and Principles of Digital Circuits Design2. Advanced Minimization Techniques3. Programmable Logic Devices (PLDs, CPLDs, FPGAs) Fundamentals4. Introduction to ASICs and ASIC Design Methodology5. Analysis, Modeling and Partitioning for Logic Synthesis and VHDL Coding6. Constraining Designs, Synthesizing, Simulation and Optimization7. Design for Testability, Built-In Self-Test, and Fault Tolerance8. Digital System Reliability9. Noise and Transmission Line Effects														
Evaluation:	<table><tr><td>Mini-Labs (3):</td><td>6 %</td></tr><tr><td>Design project:</td><td>29 %</td></tr><tr><td>Problem set (4):</td><td>0 %</td></tr><tr><td>Midterm:</td><td>20 %</td></tr><tr><td>Final exam:</td><td>45 %</td></tr></table>	Mini-Labs (3):	6 %	Design project:	29 %	Problem set (4):	0 %	Midterm:	20 %	Final exam:	45 %				
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Important Dates:	<table><tr><td>Problem Sets:</td><td>Jan 25, Feb. 8, Mar. 15, Mar. 31.</td></tr><tr><td>Project Proposal:</td><td>Jan 28, 2011</td></tr><tr><td>Mid-Term:</td><td>Mar. 1, 2011(Tentative)</td></tr><tr><td>Project Meeting:</td><td>Week of Mar. 14-18, 2011 (TBA.)</td></tr><tr><td>Project Presentation:</td><td>Week of Mar. 21-25, 2011 (TBA.)</td></tr><tr><td>Project Demo:</td><td>Week of Mar. 28-Apr.1, 2011 (TBA.)</td></tr><tr><td>Project Report:</td><td>Week of Apr. 8, 2011</td></tr></table>	Problem Sets:	Jan 25, Feb. 8, Mar. 15, Mar. 31.	Project Proposal:	Jan 28, 2011	Mid-Term:	Mar. 1, 2011(Tentative)	Project Meeting:	Week of Mar. 14-18, 2011 (TBA.)	Project Presentation:	Week of Mar. 21-25, 2011 (TBA.)	Project Demo:	Week of Mar. 28-Apr.1, 2011 (TBA.)	Project Report:	Week of Apr. 8, 2011
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Teaching Assistants:

Yi Zhang Office: EN-4031 E-mail: yz7384@mun.ca

Computer-Aided Design Tools:

Synopsys and Cadence CAD Tools for Digital System VLSI Design

Suggested Design Project Directions (not limited to):

1. General purpose and application specific processors, e.g., DLX, MIPS, DSP, and Grid Computing Processor.
2. Digital Filters.
3. Algorithms Implementations, e.g., BIST, Sorting, Routing, and Buffer Control.
4. Reconfigurable Architectures.
5. Parallel Processing

Other Notes:

1. Best Project Awards:

The best 1-2 projects (in terms of novelty, achievements, presentation, and report) will be awarded 2 bonus marks for each individual. I will sponsor selected projects for possible NECEC'11 publication from my grant.

2. Academic Dishonesty:

Academic dishonesty will not be tolerated. Reference to other people's work must be clearly specified and cited. The work in question will receive a grade of zero, and a formal process might be started. Be very careful of falling prey to plagiarism or any form of academic dishonesty.

References:

1. J. R. Armstrong, *VHDL Design Representation and Synthesis (Second Edition)*, Prentice Hall, 2000
2. M. D. Ciletti, *Advanced Digital Design with the Verilog HDL*, Prentice Hall, 2002
3. Z. Navabi, *VHDL: Analysis and Modeling of Digital Systems*, McGraw Hill (Second Edition), 1998
4. Z. Navabi, *Verilog Digital System Design*, McGraw Hill, 1999
5. S. Palnitkar, *VHDL Design Representation and Synthesis (Second Edition)*, Prentice Hall, 2000
6. P. J. Ashenden, *The Designer's Guide to VHDL*, Morgan Kaufmann Publisher, Inc, 1996
7. C. Roth, *Digital System Design Using VHDL*, PWS Publishing Co., 1998
8. S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*, McGraw Hill, 2000
9. J. Wakerly, *Digital Design: Principles and Practices (Six Edition)*, Prentice Hall, 2000
10. Yalamanchili, *VHDL Starter's Guide: From Simulation to Synthesis*, Prentice Hall, 1999
11. Neil H.E. Weste, Kamran Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley; 2nd edition; Oct 1994, ISBN: 0201533766
12. Michael J. S. Smith, *Application-Specific Integrated Circuits*, Addison-Wesley; June 1997
13. J. Bhasker, *VHDL Primer (Third Edition)*, Prentice Hall, 1999