Question 1

Draw an 8×8 Batcher-Banyan network (excluding the "trap network") and illustrate the paths taken by cells travelling between the following inputs and outputs. Indicate any blocking that might occur if the cells are switched during the same switching cycle.

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>7</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
</tr>
</tbody>
</table>

Question 2

Consider a 16×16 Banyan network. Two cells enter the switch and are to be switched during the same switching cycle.
(a) Determine the probability that there will be blocking if the output destinations are randomly selected from the 16 outputs with each output being equally likely, assuming that
   (i) the two cells arrive at inputs 4 and 5,
   (ii) the two cells arrive at inputs 0 and 11, and
   (iii) the two cells arrive at any two inputs.
(b) Assume now that the two cells come into the switch destined for outputs 4 (100) and 5 (101).
   Determine the probability, across all possible input combinations for the 2 cells, that there will be blocking. What if the cells are destined for outputs 1 and 7?

Question 3

Prove that a 4×4 Batcher merge network works.
**Question 4**

(a) Cells arrive at a purely input queued 4×4 switch. Each input port controller has one FCFS queue. The output addresses for cells arriving at the switch are given below. (For simplicity consider that each cell arrives synchronized to a cell switching cycle.) Assume that, if more than one cell is contending for an output port, the arbiter allows the cell from the lowest number input port to be switched. Determine the total delay (in switching cycles) required to switch all the packets.

(b) Repeat for a 4×4 switch which has only output queues and that is capable of storing up to 4 cells in an output queue in a switching cycle.

**Question 5**

A 4×4 packet switch is designed to switch fixed size packets. The switch fabric uses a crossbar switch fabric and has only input queues (one first-come/first-serve queue associated with each input) and no output queues. An arbiter is used to manage the scheduling of the input queues to ensure that no output blocking will occur.

Consider the following packet arrivals, where each element in the table represents the destination output.

(a) Determine the average queuing delay (i.e., time spent waiting in the queue) per packet destined for output 2. In your analysis, assume that each packet arrives synchronized to a packet switching cycle (that is, if a packet is switched immediately, it suffers no delay). Assume that the arbiter gives priority, firstly, to inputs with the most packets waiting in the queue and, secondly, to the lowest numbered input port. No packets arrive prior to cycle 1 and after cycle 4.
(b) Assume now that the switch is a broadcast bus architecture with no input queues and only output queues. Assume that the switch is capable of switching packets from the 4 inputs to any combination of outputs (i.e., up to 4 packets may be queued at an output in any switching cycle). Determine the average queuing delay for packets destined to output 2. Assume that, if there are no packets in the output queue, a packet arriving at the output may be transmitted immediately on the output link and, hence, suffers no delay.

**Question 6**

What is the largest purely output-queued ATM switch with zero cell loss requirement that we can build if we use 10 ns, 4 byte wide RAM? Assume the input lines are 155 Mbps. How large can the switch be if the memory can be accessed on a cell-wide basis? If we decide to run the output at only 0.4N times the input lines (N being the switch size) using 4 byte wide RAM, how big a switch can we build? What is the penalty paid for this scheme?

**Question 7**

Consider a 16×16 knockout switch which is capable of placing 8 cells in its buffer in any switching cycle. Assuming uniformly distributed traffic, determine an upper bound for the probability that cells will be discarded due to output blocking. The derived bound does not need to be tight, but should be non-trivial.

**Question 8**

(a) Find the cost and next hop (i.e., routing table entry) of the least cost path from node 1 to every other node for the following graph using Dijkstra's algorithm.

(b) Consider the distance vector routing approach and assume link 4-5 changes in cost from 6 to 2. Illustrate the process (i.e., the flow of information) that would result in node 1 updating its routing table.
**Question 9**

Consider the packet-switching network below with the costs associated with each link indicated. Using Dijkstra’s algorithm, find the cost and the next hop of the least-cost path from source node 1 to all other nodes in the network.

![Network Diagram](network_diagram.png)

**Question 10**

The number shown next to each link in the network below is the probability of the link failing during the lifetime of a virtual circuit from node 1 to node 7. It is assumed that links fail independently of each other.

![Network Diagram](network_diagram.png)

(a) Determine a suitable cost metric in order that a shortest path algorithm can be used to determine the most reliable path from 1 to 7 (i.e., the path with largest probability that all links will remain working).

(HINT: A shortest path algorithm minimizes a total distance which is derived by adding the length of each link. Hence, you must derive a metric for cost which is additive. You may find the fact that ln \( x \) \approx \( x - 1 \) for values of \( x \) close to 1 useful.)

(b) Find the probability of remaining intact for the most reliable path and determine the next hop from node 1 in the path.
ANSWERS:

Q1. No answer available.

Q2. (a) (i) 1/2 (ii) 1/16 (iii) 2/15
    (b) 7/15, 1/15

Q3. There are 6 scenarios that should be considered to prove that the merge works.

Q4. (a) delay = 5 cycles (b) delay = 2 cycles

Q5. (a) average delay = 8/7 cycles (b) average delay = 8/7 cycles

Q6. (a) 19x19 (b) 273x273 (c) 48x48

Q7. No answer available.

Q8. No answer available.

Q9. No answer available.

Q10. No answer available.