ECE 7500: Introduction to VLSI Design

Instructor	**Lihong Zhang**	**Teaching Assistants**	**TDB**
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Office Location	**CSF-4118**	**Office Location**	**TBD**
Office Hours	**5:00-5:30pm Thursdays** **4:00-5:30pm Fridays**	**Office Hours**	**TBD**

Website Materials for the course are posted on the course D2L site (http://online.mun.ca)

Communication *Office-hour visits or inquiries to the instructor's MUN email.*

CALENDAR ENTRY:

Introduction to VLSI Design is an introduction to ASICs and ASIC design methodology and includes basic concepts of digital logic design tools and ASIC technology libraries; partitioning for logic synthesis and VHDL coding; constraining designs, synthesizing, simulation and optimization; design for testability; layout and post-layout optimization and SDF generation; and static timing analysis.

CR: the former Computer Science 4725
LH: nine 3-hour sessions per semester
OR: eight 1-hour tutorial sessions
PR: ECE 5500

LABORATORY EXPERIENCE:
Seven laboratory experiments (including two with 6-hour sessions) are carried out by students in the course. State-of-the-art simulation and synthesis tools are used. A final lab report is written by the students.

CREDIT VALUE: 3 credits

COURSE TYPE: Elective

ACCREDITATION UNITS: 3/2.3/0.7

CONTENT CATEGORIES:

Math	Natural Science	Compl. Studies	Engineering Science	Engineering Design
			45%	55%

COURSE DESCRIPTION:

The topics will include, but not be limited to: introduction to CMOS processing technology and CMOS digital circuit and logic design; introduction to ASICs and ASIC design methodology; basic concepts about Synopsys and ASIC technology library; partitioning for logic synthesis and VHDL coding; constraining designs, synthesizing, simulation and optimization; design for testability; layout & post-layout optimization and SDF generation; static timing analysis; analog and mixed-signal integrated circuits. The course has a strong focus on engineering design, which is reflected from all of the assignments, labs, midterm, and final exam.

SCHEDULE: LECTURE: Tuesday (12:00-12:50), Thursday (12:00-12:50), Friday (13:00-13:50) Room: EN-1004
LABORATORY: Friday 14:00-17:00 Room: CSF-2112

RESOURCES:

REFERENCES

- *Michael J. S. Smith, Application-Specific Integrated Circuits, Pearson, 2011.*
- *Himanshu Bhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, Physical Compiler and Primetime, Kluwer Academic Publishers, Boston, 2002.*
- *Jan Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits, Prentice Hall, New York, 2014.*
- *Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, New York, 2017.*
- *Neil Weste and David Harris, CMOS VLSI Design, A Circuits and Systems Perspective, Addison Wesley, Boston, 2010.*
- *R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, Wiley-IEEE Press, 4 edition, 2019.*

SOFTWARE

- The software used for the labs/project includes CAD tools from Cadence, Synopsys, Mentor Graphics (now Siemens EDA), etc. To access the VLSI servers, students should obtain a VLSI account from Mr. Shannon March (smarch@mun.ca, Tel: 864-3158) in EN-3020 in the first week of the term.

MAJOR TOPICS:

- Introduction to VLSI
- Review of HDL
- Design Rules
- Coding for Synthesis

- Design with Memories, I/O Pads
- Apply Synthesis Constraints
- Synthesize the Design
- MOSFET Devices, Models of MOSFET
- Amplifiers
- CMOS Combinational Logic
- Simulate the Design
- Designing for Test
- Static Timing Analysis and Clock Tree
- Physical Design Considerations

LEARNING OUTCOMES:

Course Level Graduate Attribute Focus: KB-A, PA-A, Des.-D

Upon successful completion of this course, the student will be able to:

	LEARNING OUTCOMES	GRADUATE ATTRIBUTES. LEVEL*	Methods of Assessment
1	Demonstrate knowledge of VLSI manufacturing process and CMOS technology.	KB.3-A, KB.5-D, PA.3-D	Assignments, Midterm, Labs, Design Project, Final Exam
2	Understand the fundamentals of ASIC design methodology and basic ASIC design rules.	KB.5-A, PA.3-A, Inv.2-A, Des.1-D	Assignments, Midterm, Labs, Design Project, Final Exam
3	Design using HDL for partitioning for logic synthesis, design and I/O pads.	KB.5-A, PA.3-A, Inv.2-A, Des.3-D	Assignments, Midterm, Labs, Design Project, Final Exam
3	Apply techniques for ASIC implementation and verification process.	KB.5-A, PA.3-A, Inv.2-A, Des.3-D	Assignments, Midterm, Labs, Design Project, Final Exam
4	Use techniques for ASIC physical design, layout, and post-layout optimization.	KB.5-D, PA.3-D, Inv.2-D, Des.3-D	Assignments, Midterm, Labs, Design Project, Final Exam
5	Demonstrate knowledge of MOSFET modelling and transistor-level amplifier design.	KB.3-A, KB.5-D, PA.3-D, Inv.2-D, Des.3-D	Assignments, Midterm, Labs, Design Project, Final Exam
6	Apply ASIC design tools, technology library, and transistor-level VLSI design tools.	Tools.1-D	Midterm, Labs, Design Project, Final Exam
7	Develop ASIC design skills for fairly complex digital systems.	Inv.2-D, Des.2-D, Tools.1-D, Team.1-I	Assignments, Midterm, Labs, Design Project, Final Exam

* Each Graduate Attribute for each learning outcome is rated at a Content Instructional Level of I=Introductory, D=Developed, or A=Applied.

See http://www.mun.ca/engineering/undergrad/graduateattributes.pdf for more information on

the 12 Graduate Attributes you are expected to be proficient in upon graduation.

ASSESSMENT:

			Approximate Due Dates
Assignments	10%	(2.5% each)	
Assignment 1			May 23
Assignment 2			May 30
Assignment 4			June 8
Assignment 5			June 16
Labs	15%		
Lab 1 report			June 6
Lab 2 report			June 13
Lab 3 report			June 20
Lab 4 report			July 4
Lab 5 report			July 20
Lab final report			Aug. 4
Midterm	20%		June 23
Final exam	55%		TBA

LAB SAFETY:

Students are expected to demonstrate awareness of, and personal accountability for, safe laboratory conduct. Appropriate personal protective equipment (PPE) must be worn (e.g. steel-toed shoes, safety glasses, etc.) and safe work practices must be followed as indicated for individual laboratories, materials and equipment. Students will immediately report any concerns regarding safety to the teaching assistant, staff technologist, and professor.

ACADEMIC INTEGRITY AND PROFESSIONAL CONDUCT:

Students are expected to conduct themselves in all aspects of the course at the highest level of academic integrity. Any student found to commit academic misconduct will be dealt with according to the Faculty and University practices. More information is available at http://www.mun.ca/engineering/undergrad/academicintegrity.php

Students are encouraged to consult the Faculty of Engineering and Applied Science Student Code of Conduct at http://www.mun.ca/engineering/undergrad/academicintegrity.php and Memorial University's Code of Student Conduct at http://www.mun.ca/student/conduct/.

INCLUSION AND EQUITY:

Students who require accommodations are encouraged to contact the Glenn Roy Blundon Centre, http://www.mun.ca/blundon/about/index.php. The mission of the Blundon Centre is to provide and co-ordinate programs and services that enable students with disabilities to maximize their educational potential and to increase awareness of inclusive values among all members of the university community.

The university experience is enriched by the diversity of viewpoints, values, and backgrounds that each class participant possesses. In order for this course to encourage as much insightful and comprehensive discussion among class participants as possible, there is an expectation that dialogue will be collegial and respectful across disciplinary, cultural, and personal boundaries.

STUDENT ASSISTANCE: Student Affairs and Services offers help and support in a variety of areas, both academic and personal. More information can be found at www.mun.ca/student.