Projects Listed by Faculty Member

Spring 2009

Dr. Mohamed Hossam Ahmed
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MA1 Cooperative Wireless Networks:

Although MIMO antennas is a very promising technology for efficient transmission, the deployment of MIMO systems faces serious challenges mainly because of the limited space and power at mobile terminals (e.g, in 3G and WiMAX systems). In order to achieve the advantages of MIMO systems without installing multiple antennas at the mobile terminals, user cooperation (by relaying signals) can be utilized to implement signal diversity and spatial multiplexing. In this project we will study the implementation and performance analysis of cooperative diversity systems in multi-hop systems.

MA2 Performance of Adaptive Multi-Input Multi-Output (MIMO) Antenna Systems Over Interference-Limited Channels:

Adaptive MIMO systems are used to strike a balance between the enhancement in the signal quality (through spatial diversity) and the throughput gain (through spatial multiplexing). MIMO is a very promising technology for various wireless systems such as WLANs, WiMAX and 3G and beyond. In this project we will analyze the performance of such adaptive MIMO systems (in terms of bit error rate, throughput gain, diversity gain, etc.) over interference-limited channels.

Prof. Michael Bruce-Lockhart
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Michael Bruce-Lockhart is interested in the use of computers in education and especially in the use of visualization and animation in teaching computer programming concepts.
See him for information on projects.

Dr. Rod Byrne (Department of Computer Science)
Email: rod at cs.mun.ca, Office: EN1056

(Note that Dr. Byrne will not be supervising any projects in spring 2009.)

RB1. Op-Amp Simulator and Microcontroller controlled Op-Amp Demonstration System
The behaviour of many Op-amp circuits is controlled by the arrangement of feedback and input elements (commonly implemented with resistors).
This project has the following goals:

1) implement a microcontroller system that can configure an op-amp circuit to realize adder and difference circuits with controlled gain. Digital potentiometers can be used to configure the op-amp circuit.

2) a graphics user interface program, running on a PC, that allows a user to configure the op-amp demonstration system,
3) the microcontroller must be able to generate common waveforms (e.g., sine, square, triangle, ramp) for input to the op-amp circuit and capture the op-amp's output. The inputs and outputs should be controlled and displayed on the graphics user interface program running on the PC.

The system will allow studies to study and experiment with the behavior of common op-amp circuits. If time permits, the system should be able to realize integrator and differentiators circuits.

RB2. Web Based Logic Simulation System

Schematic circuits can down be draw by web browsers that support SVG and the canvas tag. Communication to specialized server application can be creating using the AJAX approach. The goal of this project is to create a web based system that can:

1) edit and created simple combinational logic circuits containing, AND, OR, NAND, NOR, XOR, XNOR and NOT gates.
2) simulate that output of the circuit for a given import.

The main research goal of this project is to see how easily the web based client/server architecture can be used to implement the above system. The project should also evaluate where (i.e., in the client or in the server) the functionality of the system should be realized.

RB3. A software development project: Teaching time complexity analysis though profiling of Java

Exact time complexity analysis of a program can be derived by profiling a program execution. The JVMTI interface enables the profiling and execution control of a JVM (Java Virtual Machine). The project should create a software tool using the JVMTI interface to help a student perform time complexity analysis on programs. The tool should determine and display the number of times each statement in a program was executed for a given input. The time complexity behavior of a program can determined by changes the size of the input. Similar projects are: http://yajp.sourceforge.net and http://www.ej-technologies.com/products/jprofiler/overview.html.

Dr. Octavia A. Dobre

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OD1: Exploitation of the PAPR for the Identification of the OFDM versus Single Carrier Linear Digital Modulations

Signal identification is a problem of great interest for both commercial and military communications. For example, joint signal detection and identification finds applications in emerging cognitive radio systems, whereas signal recognition is a main task of an intelligent receiver in military applications. The peak to average power ratio (PAPR) represents a drawback of the orthogonal frequency division multiplexing (OFDM) [1]. The aim of this project is to exploit PAPR as a salient feature to identify OFDM signals, and develop a

classifier based on this feature. Simulations will be performed in MATLAB to investigate the performance of the proposed classifier.

Reference:

[1] Ochiai and H. Imai, "On the distribution of the peak-to-average power ratio in OFDM signals," *IEEE Trans. Commun.*, vol. 49, pp. 282-289, Feb 2001.

OD2: Joint Signal Detection and Identification in Cognitive Radio Systems

The cognitive radio (CR) concept was first introduced by Joseph Mitola III in his doctoral dissertation, and defined as an intelligent wireless communication system, capable of sensing and adapting to its radio frequency environment [1]. CR appears to be a promising solution to the increased demand for spectrum access, efficiency and reliability in commercial wireless systems [1]-[2]. The CR central idea is to opportunistically search for and exploit the unoccupied spectrum [1]-[2]. Since a significant portion of the spectrum allocated to licensed services is sparsely occupied at any given time, such a strategy can yield major benefits [3]. Intelligent radios are also required for real-time signal interception and processing in military applications, such as spectrum surveillance and electronic warfare [4]. A major issue in such radios is the detection and classification of very low signal-to-noise ratio signals with relaxed *a priori* information on signal parameters. For more than two decades, signal cyclostationary has been explored for signal interception, modulation classification, parameter estimation, source separation, etc. [5]. Second-order cyclostationarity has been also investigated in the context of signal detection and classification for CR [6]-[7]. Recently, I have developed a joint signal detection and classification algorithm, by exploiting first-order cyclostationarity. The aim of the project is to extend this algorithm to different propagation environments. The performance of the algorithm will be verified through simulations, as well as by using collected data.

References:

[1] J. Mitola III, "Cognitive radio for flexible mobile multimedia communications," in *Proc. IEEE International Workshop on Mobile and Multimedia Communications*, 1999, pp. 3-10.

[2] S. Haykin, "Cognitive radio: brain-empowered wireless communications," *IEEE J. Select. Areas Commun.*, vol. 23, pp. 201-220, 2005.

[3] Federal Communication Commission, "Spectrum policy task force," *ET Docket* No. 02-155, Nov. 2002.

[4] O. A. Dobre, A. Abdi, Y. Bar-Ness, and W. Su, "A survey of automatic modulation classification techniques: Classical approaches and new trends," *IET Commun.*, vol. 1, pp. 137-156, April 2007.

[5] W. A Gardner, "Signal interception: a unifying theoretical framework for feature detection," *IEEE Trans. Comm.*, vol. 36, pp. 896-906, Aug. 1988.

[6] A. Tkachenko, D. Cabric, and R. W. Brodersen, "Cyclostationary feature detector experiments using reconfigurable BEE2," in *Proc. DySpan*, 2007, pp. 216-219.

[7] K. Kyouwoong, I. A. Akbar, K.K. Bae, J.-S. Um, C. M. Spooner, J. H. Reed, "Cyclostationary approaches to signal detection and classification in cognitive radio," in *Proc. DySpan*, 2007, pp. 212-215.

OD3: Signal Cyclostationarity for Biomedical Applications

Most man-made signals exhibit cyclostationarity. Second- and higher-order cyclostationarity have been exploited in digital communications for source separation, signal recognition, parameter estimation, etc. [1]-[2].

On the other hand, biological signals are generally thought to be cyclostationary. For instance, ECG and PCG signals are classified as cyclostationary signals. However, no rigorous study is available in the literature to substantiate this claim. The proposed project is to study the cyclostationarity behaviour of biological signal, especially PCG, and exploit this aspect of the signal for identifying features that would enable the classification of various components associated with this signal. Also, this project can aim to conduct binary classification of signals as normal and abnormal. The study will be conducted using simulated signals and then possibly adapted for acquired PCG signals.

References:

[1] W. Gardner, Cyclostationarity in Communications and Signal Processing. Inst Elect and Electronic Engineers, 1994.

[2] M.G. Jafari, Wang Wenwu, J.A. Chambers, T. Hoya, and A. Cichocki, "Sequential blind source separation based exclusively on second-order statistics developed for a class of periodic signals," *IEEE Trans. Sig. Proc.*, vol. 54, pp.1028 – 1040, March 2006.

Students who have their own ideas for projects in the area of signal processing for wireless communications are also encouraged to contact Dr. Dobre.

Dr. Paul Gillard (Department of Computer Science)
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PG1. Wireless distribution of local state information to a target node.

This project requires the design of both software and hardware.

The project will have several peer nodes communicating state information (time, button presses, etc.) in a wireless environment. The main problems are designing a protocol for reliable communication using low cost transceivers, the data collection at each node, and the implementation of algorithms for maintaining a consistent state at each mode. In some ways, this is similar to a small sensor network without power management.

The project will develop a real-world example, using two communicating nodes each with several inputs. A board will be designed providing appropriate input and output for the particular real-world example.

Students that have their own ideas for projects in the areas of digital hardware design and embedded systems are encouraged to contact Dr. Gillard.

Minglun Gong
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MG1. Parallel Computing on GPU/FPGA for Image Processing Applications

The graphics processing units (GPUs) on modern programmable graphics cards allow programmers to write computational kernels that are executed in parallel. Similarly, a field-programmable gate array (FPGA) allows designers to configure the semiconductor device after manufacturing. In the past few years, there are increasing number of GPU-based and FPGA-based parallel algorithms being proposed for different image processing tasks. These techniques can be much faster than the CPU-based versions, thanks to the parallel nature of image processing operations. This project will investigate how to use GPU and/or FPGA for selected image processing operations.

Dr. Howard Heys
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HH1. Digital Hardware Implementation of Ciphers Based on Data Dependent Permutations
Data dependent permutations have been proposed as a hardware-efficient operation to be used as a component within block cipher design. For example, the Cobra family of ciphers have been constructed with DDPs as their core security element. This project will involve the design and implementation of the digital hardware realization of Cobra-S128. The design will be targeted to an FPGA technology and must be implemented using a Diligent Nexys 2 development board. The outcomes of the project should include (1) a functionally tested HDL description of the cipher, (2) the synthesis of the design including an analysis of the resulting resource and timing requirements, and (3) the tested realization of the design on the Nexys 2 board.

Dr. Heys will also be interested in supervising other projects especially in the areas of cryptography and digital design.

Dr. Cheng Li
Email: licheng at engr.mun.ca, Office: EN4012
CL1 Wireless Sensor Networks: an Emulation Approach toward the Performance Evaluation of Routing and Clustering Protocols

This project involves the performance study of typical routing and clustering algorithms, such as AOVD, Heed and Leach, in wireless sensor networks through an emulation approach. The investigation will be based on Xbow Inc. Mica2 / MicaDot sensor devices and their corresponding emulation platform.

CL2. Wireless Communication in a Networked Environment

In this project, students will investigate how to conduct collision free wireless communication among many wireless devices. Different communication technologies, such as blue tooth, zigbee, and RF, will be considered and compared. The work will be based on some commercial development boards with very interested applications of those devices. Some basic communication protocol development will be involved.

CL3. Survey of Multicasting Techniques in Wireless Sensor and Mobile Ad Hoc Networks

Many multimedia network applications demand the capability of transfer information message to a number of recipients. Multicasting has been shown the most efficient approach to achieve this goal. However, multicast routing incurs significant amount of challenges due to the overhead and network dynamics. Recently, overlay multicasting and application layer multicasting has attracted much attention due to the easiness of implementation in real networks. This project involve an extensive survey of existing
mutlicasting techniques in wireless sensor and mobile ad hoc networks. For some representative algorithms, simulation will be conducted to verify some proposed schemes.

CL4. Efficient Node Discovery Scheme for Wireless Sensor Networks

In wireless sensor networks, sensor nodes are densely and randomly deployed. To turn a chaotic network into the right order for future network applications, node discovery is the first and very critical step. In this work, students will study various node discovery schemes from the literature and compare their performance. The typical ones will be picked and repeated using software simulation.

CL5. FPGA Implementation of Floating Point Number Matrix Multiplication

In this project, students will utilize existing FPGA development systems to realize floating point number matrix multiplication. The implementation will be tested and the results will be compared with those from the software implementation approach, such as in C++, Java, or Matlab.

Dr. Cecilia Moloney
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Students that have their own ideas for projects in the areas of digital signal processing and image processing are encouraged to contact Dr. Moloney.

Dr. Theodore Norvell
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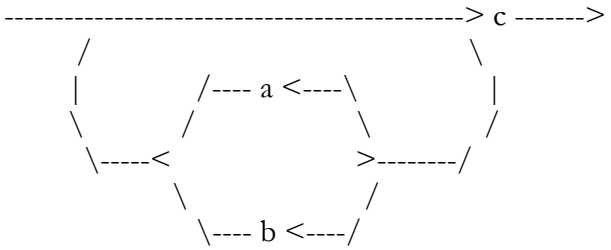
TN1. State-Chart editing and implementation

The aim is to create animations of complex systems using state-charts. We will thus create a visual editor for state-charts, an visual editor for drawing scenes, and a simulator to run the animations.•

TN2. Visual Regular Expression Editor / Visual JavaCC Editor

In a number of applications, we must edit regular expressions. For example in the JavaCC parser generator system, regular expressions are used (with slightly different syntaxes) to specify the lexical syntax and grammatical syntax of a language. A nice graphical syntax for regular expressions is a "rail-road" diagram — a sort of a state-diagram or flow-chart.

A nice tool would be an editor for a language like JavaCC in which the lexical and grammatical components are specified using a visual editor for regular expressions displayed as railroad diagrams.
Here is an ascii version of a rail-road diagram for (a|b)*c



Next steps: I would an editor for JavaCC structured into three layers. The first layer would be a framework for editing structured (hyper-)graphs. This is the deep model layer. The second layer is a surface model. This would be build on the first, but also on JGraph. The third layer would apply the second layer to a specific language (JavaCC). These three layers could be split into 1 or 2 projects depending ambition and available students.

TN3. A HARPO/L to Java or C translator.

HARPO/L is a parallel object-oriented language intended for hardware/software codesign. Programs written in HARPO/L can be run on either programmable hardware (CGRAs and FPGAs) or on microprocessors. For programs written in HARPO/L to run on microprocessors we will translate it to a language such as Java or C that has existing compilers.

Students that have their own ideas for projects in the areas of software engineering, formal approaches to software engineering, hardware design languages, and programming languages are encouraged to contact Dr. Norvell.

Dr. Siu O'Young
Email: oyoung at engr.mun.ca, Office: EN3074

See Dr. O'Young about project ideas in discrete controls and autonomous aircraft and other interesting areas.

Dr. Dennis Peters
Email: dpeters at engr.mun.ca, Office: EN3061

Dr. Peters has many exciting ideas that he will be happy to explain to you.

Dr. Andrew Vardy
Email: avardy, Office: EN2018

AV1. Visual Simultaneous Localization and Mapping

Simultaneous Localization and Mapping (SLAM) of mobile robots is typically accomplished by active-ranging sensors such as laser rangefinders. Recently, the use of visual ranging has been applied to this problem. The goal of this project is to develop a system to solve the SLAM problem using stereo vision. Prerequisite: Computer Science 6778.

AV2. Vector Mapping for Mobile Robot Navigation

A robot that has been displaced from a goal location has the task of returning to the goal using vision. This task is known as "visual homing". One means of achieving visual homing is for the robot to record a "snapshot image" taken when at the goal and later to use the disparity between the currently-viewed image and the snapshot image to guide the robot back to the goal. Feature-based approaches to this problem attempt to find correspondences between features in the snapshot image with features in the current image. Once these correspondences have been established they can be used to compute a home vector. This process is known as "vector mapping". The goal of this project would be to investigate methods for vector mapping that are able to cope with many incorrect correspondence vectors. In particular, the use of the RANSAC algorithm for this process would be investigated. Prerequisite: Computer Science 6778.

Dr. R. Venkatesan
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RV1. Development of cache snooper hardware using the MESI protocol
This project is suitable for someone interested in computer hardware, VHDL and FPGA.

RV2. Development of cache snooper hardware using the dragon protocol
This project is suitable for someone interested in computer hardware, VHDL and FPGA.

RV3. Hardware development of a cache controller
This project involves design, VHDL implementation and testing of a real cache; L1 cache using 2-way set-associativity, alternate block replacement policy, write-through strategy with a write buffer, write no-allocate strategy, way prediction and line prediction, and is suitable for someone interested in computer hardware, VHDL, SoC and FPGA.

Dr. Fang Wang
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FW1. Minicomputer design and verification
The goal of this project is to simulate the design of a digital system. With the functional description of the system, the designer usually constructs a Register Transfer Level (RTL) model which should be checked to ensure it meets all requirements. This project consists of two phases: first design a minicomputer with pipelined CPU and then verify the design with SMV (a formal verification tool). The minicomputer consists of a memory, a CPU (registers, ALU, stack), and the system bus. The CPU fetches instructions from the memory, interprets them and executes the operations, and stores the results into memory when needed. It is assumed that the memory can be accessed in one clock cycle and works

synchronously with the CPU. The CPU design is in a pipeline architecture consisting of controller and data path. This project requires computer architecture background and using SMV with minor supervision.

FW2: Formal verification of an ATM design
Asynchronous Transfer Mode (ATM) is a cell relay, packet switching network and data link layer protocol which encodes data traffic into small fixed-sized cells. This project deals with modeling and verifying an ATM network component -- the Fairisle 4 by 4 switch fabric. The device is a part of the Fairisle ATM network designed and in use at the Computer Laboratory of the University of Cambridge. This switch fabric was fabricated without consideration for formal verification. Thus, this project will model this device with hardware design languages such as Verilog and then verify the model with a verification tool, where techniques of reduction and abstraction should be applied to deal with state space explosion. This project requires some knowledge of formal verification methods and the experience of verification tools.

FW3: Verification of wireless communication protocols using SPIN
SPIN is a model checker developed in Bell Labs targeting efficient software verification. Spin has been used to trace logical design errors in distributed systems design, such as operating systems and communications protocols. This project is to model wireless communication protocols such as IEEE802.11 and IEEE802.16 using PROMELA and then check the model with SPIN. The knowledge and experience of SPIN are necessary.

Dr. Lihong Zhang
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LZ1. Design and analysis of VLSI electronic design automation algorithms

Due to the rapid evolution of integrated circuit (IC) technology, the number of transistors on a single chip has grown from a few to over hundreds of million. The design and fabrication of Very-Large Scale Integration (VLSI) chips have developed beyond the capabilities of any number of humans without computer support. That is why Electronic Design Automation (EDA) tools are widely used in the modern VLSI design. This project is a software-oriented one, where students can choose one EDA topic (such as netlist sizing, partition, placement, routing, etc). The work includes a literature survey of available algorithms published recently, algorithm analysis/design, and software implementation in object-oriented languages. If time permits, some experiments will be conducted using certain benchmark circuits followed by comparison study.

LZ2. Extraction of modern MOSFET models for bulk-driven applications

Conventionally a MOSFET is used as a three-terminal (i.e., *gate*, *source* and *drain*) device called a gate-driven MOSFET, where a signal is input from the *gate* terminal and the *bulk* terminal is simply connected to power or ground. As a promising technique, a MOSFET can be used as a four-terminal device (i.e., *bulk* additionally) and the signal can be input from the bulk terminal. As most of the modern MOSFET models used in the commercial simulators of the advanced submicron and nano technology are adapted for gate-driven MOSFETs, we want to study their performance in the bulk-driven applications. In this project, you will use some

state-of-the-art commercial tools to extract MOSFET models. You can learn how to run VLSI transistor-level simulation. The target technology is CMOS 90nm. Based on the extracted models, gate-driven and bulk-driven simulations can be run to compare the performance of multiple models.

LZ3. Design and optimization of low-power low-voltage mixed-signal integrated circuits

It is predicted that over 80 percent of all integrated circuits (ICs) would include mixed signals, compared to about 25 percent five years ago. This project is to investigate strategies that can be used to design and optimize low-power low-voltage mixed-signal ICs. Students will learn how to run transistor-level simulation and basic design techniques. The major work will include literature survey, background buildup, circuit design, and simulation verification. Some candidate topics may be ultra low-power digital logic, picoammeter circuits, or MEMS applications.

LZ4. Complete FPGA implementation of digital systems

This project is to design and implement a digital system, such as a decoder or operator, using our existing FPGA development environment. This will contain the full design flow of the SoC design process, including RTL design, logic synthesis, and physical synthesis. The chosen digital system is not necessarily complex. The key points of this project are: 1) getting the entire flow work correctly; 2) choosing and correctly configuring the FPGA placement and routing tools; 3) investigating the utilization problem of the chosen FPGA placement tool.

LZ5. ASIC design and implementation of digital systems

This project is to design and implement a digital system using the recommended ASIC design flow and methodology supported by Canadian Microelectronics Corporation (CMC). The complete flow will include architecture design, RTL design, logic synthesis, and physical synthesis (i.e., placement and routing). The chosen digital system is not necessarily complex. The target technology is CMOS 0.13 um or 0.18 um. It is possible for a successful design/implementation to be fabricated after the project is done.