1

a) CPU_time_original

$= IC \times Clock\ Cycle \times (2 + 100\% \times 1\% \times 25 + 28\% \times 5\% \times 25)$

$= 2.6 \times IC \times Clock\ Cycle$

CPU_time_modified

$= IC \times Clock\ Cycle \times (2 + 100\% \times 1\% \times 25 + 20\% \times 5\% \times 25 + 8\% \times 10\% * 25)$

$= 2.7 \times IC \times Clock\ Cycle$

Percentage change = (2.7-2.6)/2.6 = 3.85 %

b) IC = 300,000, Clock cycle = $1 / 600*10^6$

CPU_time_ modified = $2.7 * 300{,}000 * 1 / 600*10^6$ = 0.0014 **s**

CPU_time_original = $2.6 * 300{,}000 * 1 / 600*10^6$ = 0.0013 s

# of times of modified mode = 1 / 0.0014 = 714.2857

# of times of original mode = 1 / 0.0013 = 769.2308

c) Average_CPU_time

= hittimeL1 + missrateL1*(hittimeL2 +missrateL2 * misspenaltyL2)*Clock Cycle

$=( 2 + (100\% * 1\% + 20\% * 5\% + 8\% * 10\%) \times (15 + 20\% * 25) ) * 1 / 600*10^6$

$= 2.56 * 1 / 600*10^6$

= 4.2667e-009 s

d) Average_CPU_time

= hittimeL1 + missrateL1*(hittimeL2 +missrateL2 * misspenaltyL2)*Clock Cycle

misspenaltyL2 = (hittime_mainmem +missrate_mainmem * misspenalty_mainmem)

Average_CPU_time =

$$\left( \begin{array}{l} 2 + \\ (100\% * 1\% + 20\% * 5\% + 8\% * 10\%) \\ * (15 + 20\% * (25 + 0.0005\% * 8 * 10^{-3} / (1/600 * 10^6))) \end{array} \right) * clcokcycle$$

$= 2.6944 * 1 / 600*10^6$

= 4.4907e-009 s

3

a) IC = 2

# 0f blocks = 128 k / 64 = $2^{11}$ = 2048

# 0f memory access = 128 * 1024 * 1500 / 8 = 24576000

# 0f instruction access = 128 * 1024 * 1500 * 2 / 8 = 49152000

# of pages = 128 k / 16 k = 8

DTLB = 8 / 24576000 = 3.2552e-007

ITLB = 1 / 49152000 = 4.0690e-008

Dcache_L1= 2048 * 1500 / 24576000 = 0.1250

Icache_L1 = 2 / 49152000 = 8.1380e-008

cache_L2= (2048 + 2) / (24576000 +2) = 8.3415e-005

CPU_time

= 49152000 * 1 + 2 * (10 + 40) //instruction access time

+ 24576000 * 1 + 2048 * (10 + 40) + 2048 * 1499 * 10 // data access time

= 104530020 clock cycles

b) instruction will be missed for each time.